

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-195655

(43)Date of publication of application : 21.07.1999

(51)Int.Cl. H01L 21/337  
H01L 29/808  
H01L 29/78

(21)Application number : 10-000665

(71)Applicant : FUJI ELECTRIC CO LTD

(22)Date of filing : 06.01.1998

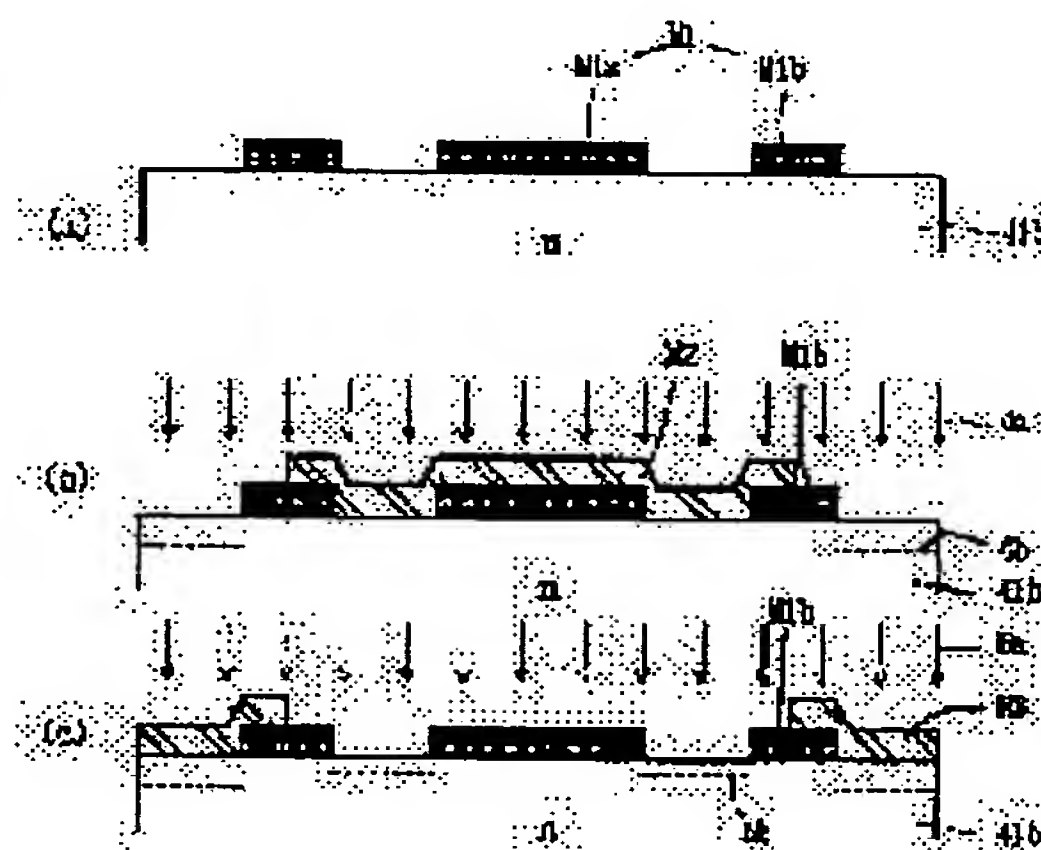
(72)Inventor : UENO KATSUNORI

## (54) MANUFACTURE OF VERTICAL SILICON CARBIDE FET AND VERTICAL SILICON CARBIDE FET

## (57)Abstract:

**PROBLEM TO BE SOLVED:** To provide a very precise channel having a high breakdown strength by forming each impurity introducing area in a self-aligning way, by specifying each impurity introducing area with the partial end and the other part of one mask of a plurality of masks by using another mask partially overlapping the mask.

**SOLUTION:** After a polycrystalline silicon film is deposited on the surface of an n-type drift layer 41b, a mask M1 is formed by patterning this silicon film. The mask M1 is composed of a central section M1a and both side sections M1b. Then, after an SiO<sub>2</sub> film is deposited on the mask M1 and a mask M2 is formed by patterning the SiO<sub>2</sub> film, source regions are formed by implanting ions 4a which become an n-type impurity into the regions regulated by the masks M1 and M2. The mask M2 can be easily aligned with the mask M1, because no further alignment is required when the end of the mask M2 is on the mask M1. After the mask M2 is removed and a mask M3 is formed by again forming a pattern, p-type gate region is formed by injecting ions 5a which becomes a p-type impurity into the region regulated by the masks M1 and M3.



## LEGAL STATUS

[Date of request for examination] 27.01.1999

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3216804

[Date of registration] 03.08.2001

[Number of appeal against examiner's decision]

of rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

(19) 日本国特許庁 (J P)

(12) 公 開 特 許 公 報 (A)

(11) 特許出願公開番号

特開平11-195655

(43) 公開日 平成11年(1999) 7月21日

(51) Int.Cl.<sup>8</sup>

識別記号

H 0 1 L 21/337  
29/808  
29/78

F I

H 0 1 L 29/80  
29/78

C

6 5 2 T  
6 5 4 Z

審査請求 有 請求項の数19 O L (全 18 頁)

(21) 出願番号 特願平10-665

(22) 出願日 平成10年(1998) 1月6日

(71) 出願人 000005234

富士電機株式会社

神奈川県川崎市川崎区田辺新田1番1号

(72) 発明者 上野 勝典

神奈川県川崎市川崎区田辺新田1番1号

富士電機株式会社内

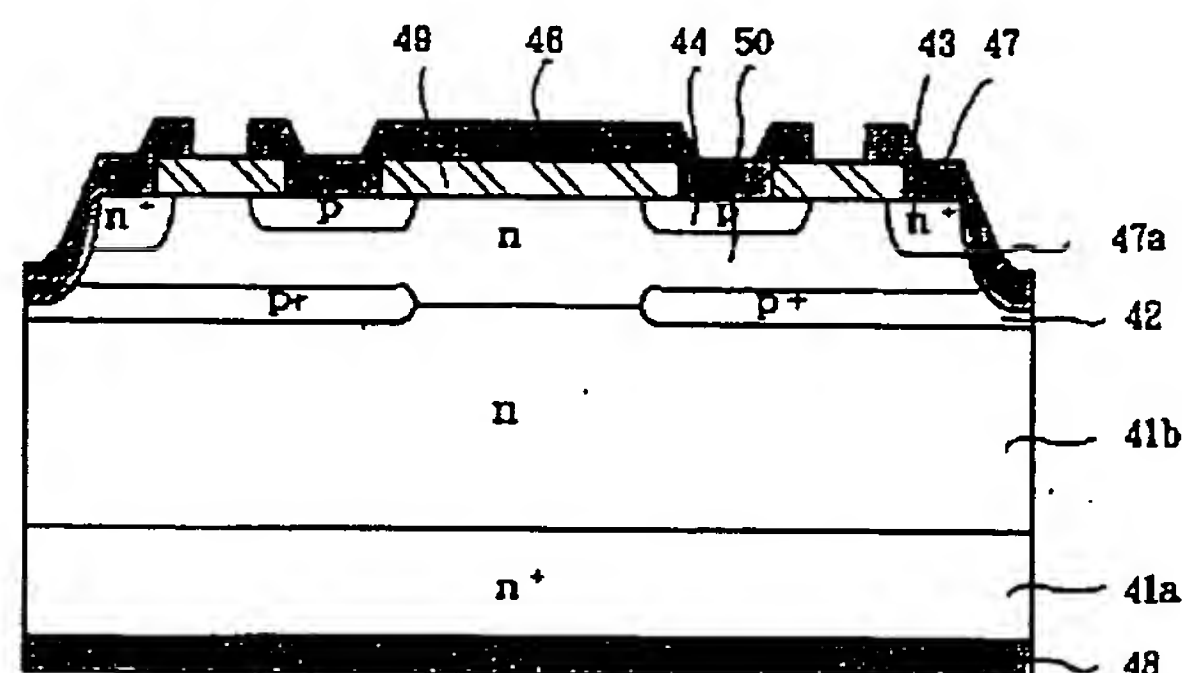
(74) 代理人 弁理士 篠部 正治

(54) 【発明の名称】 炭化けい素縦形F E Tの製造方法および炭化けい素縦形F E T

(57) 【要約】

【課題】 非常に精密で均一なチャネルが実現でき、かつ容易に高耐圧できるS i Cを用いた縦形のF E Tの製造方法を提供する。

【解決手段】 第一のマスクと一部重複する第二のマスクとを用いて第一のマスクの一部の一方の端により第一導電型不純物導入領域を規定し、第一のマスクの一部および第二のマスクを除去して第一のマスクの別の部分により第二導電型不純物導入領域を規定することによって、第一導電型不純物導入領域および第二導電型不純物導入領域を自己整合的に形成する。また、端部をテーパー状にしたマスクを用い、加速電圧を変えてイオン注入する方法を取れば、一枚のマスクだけで、第一導電型不純物導入領域および第二導電型不純物導入領域を自己整合的に形成する。特に、チャネル領域の不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのF E Tとすることができる。



41a n<sup>+</sup> ドレイン層

41b n ドリフト層

42 p<sup>+</sup> 埋め込み領域

43 n<sup>+</sup> ソース領域

44 p ゲート領域

45 ゲート電極

47 ソース電極

47a 凹部

48 ドレイン電極

49 絶縁膜

50 n チャネル領域

## 【特許請求の範囲】

【請求項1】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に互いに隔離して形成された第二導電型ゲート領域、第一導電型ソース領域と、その第二導電型ゲート領域および第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第二導電型ゲート領域の表面に接触して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形FETの製造方法において、第一のマスクの一部の一方の端により第一導電型ソース領域の一方の端を規定し、第一のマスクの一部の他方の端と第一のマスクの他の部分とにより第二導電型ゲート領域を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定してそれぞれの領域を形成することを特徴とする炭化けい素縦形FETの製造方法。

【請求項2】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなる炭化けい素縦形FETの製造方法。

【請求項3】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、そ

れらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第二導電型埋め込み領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなる炭化けい素縦形FETの製造方法。

【請求項4】第一導電型ソース領域、第二導電型ゲート領域、第二導電型埋め込み領域形成のための不純物の導入がいずれもイオン注入によっておこなわれることを特徴とする請求項2または3に記載の炭化けい素縦形FETの製造方法。

【請求項5】第一導電型ドリフト層の表面とショットキー接合を形成する電極を設けることを特徴とする請求項1ないし4のいずれかに記載の炭化けい素縦形FETの製造方法。

【請求項6】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形FETの製造方法において、第一のマスクの一部により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定することを特徴とする炭化けい素縦形FETの製造方法。

【請求項7】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入



する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、残した第一のマスクの一部を除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレータに接触するドレイン電極を形成する工程とからなる炭化けい素縦形 FET の製造方法。

【請求項 8】第一導電型炭化けい素サブストレータ上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型埋め込み領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆する工程と、その絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレータに接触するドレイン電極を形成する工程とからなる炭化けい素縦形 FET の製造方法。

【請求項 9】第一導電型炭化けい素サブストレータ上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型ベース領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられ

たソース電極と、炭化けい素サブストレータの裏面に設けられたドレイン電極とを有する縦形 FET の製造方法において、端部がゆるやかなテーパ状の第一のマスクの厚さの厚い部分により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの第一のマスクの厚さの薄い部分により第二導電型ベース領域の端を規定することを特徴とする炭化けい素縦形 FET の製造方法。

【請求項 10】第一導電型炭化けい素サブストレータ上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に端部がゆるやかなテーパ状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、第一のマスクの厚さの薄い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレータに接触するドレイン電極を形成する工程とからなる炭化けい素縦形 FET の製造方法。

【請求項 11】第一導電型炭化けい素サブストレータ上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に端部がゆるやかなテーパ状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、第一のマスクを除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部を形成する工程と、絶縁

膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレートに接触するドレイン電極を形成する工程とからなる炭化けい素縦形FETの製造方法。

【請求項12】第一のマスクの側方にサイドウォールを設け、第一のマスクとそのサイドウォールとを第三のマスクとすることを特徴とする請求項10または11に記載の炭化けい素縦形FETの製造方法。

【請求項13】第二導電型ベース領域に達する第二導電型コンタクト領域形成のための厚さの厚い第三のマスクを形成する工程と、そのマスクにより不純物を導入する工程を先に経た後、その第三のマスクをエッチバックして端部がゆるやかなテーパ状の第一のマスクとすることを特徴とする請求項9ないし11のいずれかに記載の炭化けい素縦形FETの製造方法。

【請求項14】第一導電型ソース領域、第二導電型埋め込み領域、第二導電型ベース領域形成のための不純物の導入がいずれもイオン注入によっておこなわれることを特徴とする請求項6ないし13のいずれかに記載の炭化けい素縦形FETの製造方法。

【請求項15】第一導電型ドリフト層の表面層の全面にチャネル領域の不純物濃度制御のための第一導電型不純物を導入する工程が加えられていることを特徴とする請求項1ないし14のいずれかに記載の炭化けい素縦形FETの製造方法。

【請求項16】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に少なくとも一部が埋め込まれて形成された第二導電型ベース領域と、その第二導電型ベース領域の上方の一部に第二導電型ベース領域と接して形成された第一導電型ソース領域と、第二導電型ベース領域上に残された第一導電型ドリフト層であるチャネル領域上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形FETにおいて、第二導電型ベース領域の端部の接合深さが第一導電型ソース領域から遠ざかる程ほぼ直線的に浅くなることを特徴とする炭化けい素縦形FET。

【請求項17】第二導電型ベース領域と一部が重複するように、第二導電型ベース領域より高不純物濃度で、第二導電型ベース領域より接合深さの深い第二導電型コンタクト領域が設けられ、その第二導電型コンタクト領域の表面にソース電極が接することを特徴とする請求項16記載の炭化けい素縦形FET。

【請求項18】第二導電型コンタクト領域が埋め込まれて設けられ、第一導電型ソース領域の表面から第二導電

型コンタクト領域に達する凹部が設けられて、第二導電型コンタクト領域の露出表面にソース電極が接することを特徴とする請求項16記載の炭化けい素縦形FET。

【請求項19】チャネル領域の不純物濃度が、第一導電型ドリフト層のそれより高濃度であることを特徴とする請求項16ないし18のいずれかに記載の炭化けい素縦形FET。

【発明の詳細な説明】

【0001】

10 【発明の属する技術分野】本発明は、半導体材料として炭化けい素を用いた、電力用半導体素子である接合型または金属-酸化膜-半導体構造のMOS型のゲートをもつ縦型電界効果トランジスタ（以下FETと記す）の製造方法および縦型電界効果FETに関する。

【0002】

【従来の技術】炭化けい素（以下SiCと記す）は、バンドギャップが広く、また最大絶縁電界がシリコン（以下Siと記す）と比較して約一桁大きいことから、次世代の電力用半導体素子への応用が期待されている材料である。これまでに、4H-SiCまたは6H-SiCと呼ばれる単結晶ウェハを用いて様々な電子デバイスへ応用されつつあり、特に高温、大電力用素子に適すると考えられている。上記の結晶は閃亜鉛鉱型とウルツ鉱型とを積層した形のアルファ相SiCである。他に3C-SiCと称されるベータ相SiCの結晶でも半導体装置が試作されている。最近では電力用素子としてショットキーダイオード、縦形MOSFET、サイリスタなど、あるいは最も汎用的な半導体装置であるCMOS-ICが試作され、その特性から従来のSi半導体装置と比較して非常に特性が良好なことが確認されている【例えば、Weitzel, G.W. 他：IEEE Trans. on Electron Devices, vol. 43, No. 10, pp. 1732-1741 (1997)】。MOSFETの幾つかの例を以下に示す。

30

40

50

【0003】図13は高周波素子の一つとして開発されている接合型FET（以下JFETと略す）の単位セルの部分断面図である[Sheppard, S.T. 他, Abstracts of Int. Conf. on Silicon Carbide, III-Nitrides and Related Materials, (1997)]。p<sup>+</sup>基板10上に積層されたnドリフト層11の表面層にn<sup>+</sup>ソース領域13、pゲート領域15、n<sup>+</sup>ドレイン領域が形成されている。n<sup>+</sup>ソース領域13、n<sup>+</sup>ドレイン領域14、pゲート領域15に接触してそれぞれ、ソース電極17、ドレイン電極18、ゲート電極16が設けられている。

【0004】この構造では、ゲート電極16に電圧を印加すると、pゲート領域15からpゲート領域15とp<sup>+</sup>基板10との間のnチャネル領域20に空乏層が広がる。これによってソース電極17とドレイン電極18との間の電流が抑制される。また、ゲート電極16に印加された電圧を取り去ることによって、ドレイン電極18とソース電極17との間に再び電流が流れる。このよう



にソース・ドレイン間の電流はゲート電圧によってスイッチング可能な素子となっている。このJFETは、ゲート電極16への電圧印加によってチャネル領域を空乏化するので、デプレッション型と呼ばれる。表面からp<sup>+</sup>基板10に達する溝が形成され、絶縁膜19が充填されているのは、素子分離のためである。

【0005】一方、図14は縦型MOSFETの1種である[Shenoy, J.N. 他, Abstracts of Int. Conf. on Silicon Carbide, III-Nitrides and Related Materials, (1997)]。n<sup>+</sup>サブストレータ21a上に積層されたnドリフト層21bの表面層に高加速電圧のイオン注入によりp<sup>+</sup>埋め込み領域22を形成する。そのp<sup>+</sup>埋め込み領域22の上のnドリフト層部分21bの表面層にn<sup>+</sup>ソース領域23が形成されている。二つのn<sup>+</sup>ソース領域23に挟まれたnドリフト層部分21bの表面上にゲート絶縁膜25を介してゲート電極26が設けられている。n<sup>+</sup>ソース領域23の表面にソース電極27が、n<sup>+</sup>サブストレータ21aの裏面にドレイン電極28がそれぞれ設けられている。

【0006】この例ではゲート部分がpn接合ではなく、ゲート絶縁膜25を介して電圧を印加するMOS構造になっている。このMOSFETにおいては、ゲート電極層26に正電圧を印加することによって、ゲート電極26直下のnドリフト層21bの表面部分のnチャネル領域30に蓄積層が誘起され、ドレイン電極28と、ソース電極27との間に電流が流れる。また、ゲート電極26に負電圧を印加すれば、ドレイン電極28とソース電極27との間の電流を遮断することができ、スイッチング機能を有す。ソース・ドレインの間の電圧はp<sup>+</sup>埋め込み領域22およびnドリフト層21bの間に印加されて大きな電圧を保持することが可能であり、高耐圧に適した構造にしたものである。このMOSFETは、ゲート電極26への電圧印加によって蓄積層を形成するので、ACCUFETと呼ばれる。

【0007】図15は別の縦型高耐圧MOSFETの単位セルの部分断面図である[Onda, S. 他, Phys. Stat. Sol. (a), vol. 162, p. 369, (1997)]。n<sup>+</sup>サブストレータ31a上に積層されたnドリフト層31bの表面層にpベース領域32が形成され、そのpベース領域32の表面層にn<sup>+</sup>ソース領域33が形成されている。二つのn<sup>+</sup>ソース領域33をつなぐnチャネル領域40がエピタキシャル成長により形成されており、そのnチャネル領域40の表面上にゲート絶縁膜35を介してゲート電極層36が設けられている。n<sup>+</sup>ソース領域33の表面にソース電極27が、n<sup>+</sup>サブストレータ31aの裏面にドレイン電極38がそれぞれ設けられている。

【0008】この場合も、ゲート電極層36に正電圧を印加することによって、ゲート電極層36直下のnチャネル領域40の表面部分に蓄積層が誘起され、ドレイン電極38から、ソース電極37への電流を流すことが可

能となる。また、ゲート電極層36に負電圧を印加することによって、ドレイン電極38とソース電極27との間が遮断されて、スイッチング機能を示すことになる。

【0009】他に、プレーナ型、或いはトレンチ型のMOSFETの試作例もあるが、SiCでは反転層の移動度が非常に小さいことが実験的にわかっており、反転層を用いるエンハンスメント型のFETは実用に適さないと考えられる。それに対し、上記三例の素子は反転層を用いるエンハンスメント型のFETではなく、もともとの導電型の半導体層をチャネルとして用いたFETであるという点で共通の特徴をもち、特にSiCに適する構造の例である。

【0010】

【発明が解決しようとする課題】電力用の半導体素子を製造しようとするとき、図13、14や図15の構造は非常に優れた特性が期待されるものの、実際にはこれまであまり良好な特性が実現していないか、または実際には製造されていない。その理由の一つは、Si半導体でもっとも普及している方法である二重拡散MOS(D-MOS)構造が、SiCでは容易に実現できない点にある。

Siでは、p型不純物とn型不純物とを同一のマスクにより選択的に導入し、熱拡散することによって、精密なチャネル密度が実現される。すなわちMOSFETの特性を左右するチャネルの寸法が、非常に精密に制御可能で、歩留まり良くMOSFETを作ることができる。

【0011】これにに対し、SiCではイオン注入した不純物の活性化率が悪く、これを向上させるために、1000℃以上でのイオン注入、また1600℃以上での活性化熱処理が必要であり、また、イオン注入した不純物の拡散がほとんど起きない。そのため、p型不純物とn型不純物の導入とをそれぞれ別々のマスクによらねばならず、精密なチャネル密度の制御が実現されない。そのため、チャネル抵抗が大きく、またそのバラツキも非常に大きなものとなって、素子全体の抵抗はほぼチャネル抵抗で規定されてしまう程である。SiC本来の特性が得られていないといえる。

【0012】以上の問題に鑑み本発明の目的は、非常に精密なチャネルが実現でき、かつ容易に高耐圧できる炭化けい素縦型FETの製造方法および炭化けい素縦型FETを提供することにある。

【0013】

【課題を解決するための手段】上記課題解決のため本発明は、第一導電型炭化けい素サブストレータ上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に互いに隔離して形成された第二導電型ゲート領域、第一導電型ソース領域と、その第二導電型ゲート領域および第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第二導電型ゲート領域の表面に接触して設けられたゲート電極層と、第一導電型ソース領域と第二導

電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレーートの裏面に設けられたドレイン電極とを有する縦形FETの製造方法において、第一のマスクの一部の一方の端により第一導電型ソース領域の一方の端を規定し、第一のマスクの一部の他方の端と第一のマスクの他の部分とにより第二導電型ゲート領域を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定するものとする。

【0014】例えば、具体的な工程としては、第一導電型炭化けい素サブストレーート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【0015】そのようにすれば、チャンネル領域の実質的な寸法は、第二導電型ゲート領域で決まるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。これにより、オン抵抗の小さいFETを製造することが可能である。第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成してソース電極を設ける代わりに、第二導電型埋め込み領域に達する第二導電型コンタクト領域を形成してもよい。そのようにすれば、表面上にソース電極を設けることができる。

【0016】特に、第一導電型ソース領域、第二導電型ゲート領域、第二導電型埋め込み領域形成のための不純物の導入がいずれもイオン注入によっておこなわれるものとすれば、SiCにおいても確実に不純物領域の形成ができる。第一導電型ドリフト層の表面とショットキー接合を形成する電極を設けてもよい。

【0017】そのようにすれば、接触抵抗のために必要

な第二導電型ゲート領域の寸法より、小さなチャンネル領域とすることができる。また、第一導電型炭化けい素サブストレーート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレーートの裏面に設けられたドレイン電極とを有する縦形FETの製造方法において、第一のマスクの一部により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定するものとする。

【0018】例えば、具体的な工程としては、第一導電型炭化けい素サブストレーート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、残した第一のマスクの一部を除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【0019】この場合も、チャンネル領域の寸法は、第一のマスクで決められるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成してソース電極を設ける代わりに、第二導電型埋め込み領域に達する第二導電型コンタクト領域を形成してもよい。そのようにすれば、表面上にソース電極を設けることができる。

【0020】別の方法として、端部がゆるやかなテーパ状の第一のマスクの厚さの厚い部分により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの第一のマスクの厚さの薄い部分により第二導電型ベース領



域の端を規定することもできる。例えば、具体的な工程としては、第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、端部がゆるやかなテーパー状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、第一のマスクを除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【0021】この場合もチャネル領域の寸法は、第一のマスクで決められるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。しかも、不純物領域形成のための別のマスクを必要としない。第一導電型ソース領域の表面から第二導電型ベース領域に達する凹部を形成し、第一導電型ソース領域と、第二導電型コンタクト領域に接触するソース電極を設けても良い。

【0022】特に、第一のマスクの側方にサイドウォールを設ける工程と、第一のマスクとサイドウォールをマスクとして、第二導電型コンタクト領域形成のための不純物導入工程が加えられているとよい。そのようにすれば、マスク合わせによらず、第二導電型ベース領域とずらした第二導電型コンタクト領域の形成ができる。

【0023】第二導電型コンタクト領域形成のための厚さの厚い第三のマスクを形成し、そのマスクにより不純物を導入する工程を先に経た後、その第三のマスクをエッチバックして端部がゆるやかなテーパー状の第一のマスクとすることができる。そのようにすれば、第一のマスクと第三のマスクとはもとは同じものであり、別のマスク材料を形成する必要が無い。

【0024】更に、第一導電型ソース領域、第二導電型埋め込み領域、第二導電型ベース領域形成のための不純物の導入がいずれもイオン注入によっておこなわれるものとすれば、SiCにおいても確実に不純物領域の形成ができる。そして、第一導電型ドリフト層の表面層の全面にチャネル領域の不純物濃度制御のための第一導電型不純物を導入する工程が加えられているものとする。

【0025】チャネル領域の不純物濃度を制御すること

によって、しきい電圧を制御することができ、また、ノーマリオフのFETとすることができる。上記のような製造方法により、第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に少なくとも一部が埋め込まれて形成された第二導電型ベース領域と、その第二導電型ベース領域の上方の一部に第二導電型ベース領域と接して形成された第一導電型ソース領域と、第二導電型ベース領域上に残された第一導電型ドリフト層であるチャネル領域上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有し、第二導電型ベース領域の端部の接合深さが第一導電型ソース領域から遠ざかる程ほぼ直線的に浅くなる炭化けい素縦形FETとすれば、チャネル領域の長さの制御が容易であり、均一なチャネル領域を持つ縦形FETが容易に製造できる。

【0026】第二導電型ベース領域と一部が重複するように、第二導電型ベース領域より高不純物濃度で、第二導電型ベース領域より接合深さの深い第二導電型コンタクト領域を設け、その第二導電型コンタクト領域の表面にソース電極を接触させても、第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部が設けられて、第二導電型コンタクト領域の露出表面にソース電極を接触させても良い。

【0027】第一導電型ソース領域と同じ表面で第二導電型コンタクト領域の表面にソース電極を接触させれば、凹部を設ける必要が無く、第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部を設けてソース電極を接触させれば、第二導電型コンタクト領域の厚さを厚くする必要が無い。チャネル領域の不純物濃度が、第一導電型ドリフト層のそれより高濃度であるものとすれば、不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのFETとすることができる。

【0028】

【発明の実施の形態】以下本発明について、実施例を示しながら詳細に説明する。ただし、図13～15と共通の部分、あるいは本発明とかかわりのない部分については説明を省略する。本発明の重要な応用例としてnチャネルMOSFETを例に取っているが、導電型を逆にしたpチャネルMOSFETにも本発明が適応可能なことは勿論である。なお、ここで説明する炭化けい素は良く知られているように、多くのポリタイプが存在するが、主に6Hおよび4Hと呼ばれるものを対象としている。

【0029】〔実施例1〕図1は本発明第一の実施例（以下実施例1と記す。以下同様）にかかるSiCJFETの単位セルの断面図である。これは図13の従来素子を高圧化した素子に対応している。n<sup>+</sup>サブストレ

ート41a上にエピタキシャル成長によりnドリフト層41bが積層されたウェハにおいて、nドリフト層41bの表面から少し深い位置にp<sup>+</sup>埋め込み領域42が形成され、p<sup>+</sup>埋め込み領域42の上方のnドリフト層41bの表面層にはpゲート領域44とn<sup>+</sup>ソース領域43とが形成されている。pゲート領域44の表面上にはゲート電極46が設けられている。n<sup>+</sup>ソース領域43の表面から掘り下げられた凹部47aの表面に沿って、n<sup>+</sup>ソース領域43とp<sup>+</sup>埋め込み領域42との表面に共通に接触してソース電極47が設けられ、またn<sup>+</sup>サブストレータ41aの裏面に接触してドレイン電極48が設けられている。

【0030】主なディメンジョンの一例は、次のような値である。n<sup>+</sup>サブストレータ41aの不純物濃度は $1 \times 10^{18} \text{ cm}^{-3}$ 、厚さ $350 \mu\text{m}$ 、nドリフト層41bのそれは、 $1 \times 10^{16} \text{ cm}^{-3}$ 、厚さ $10 \mu\text{m}$ 。p<sup>+</sup>埋め込み領域42の最高不純物濃度は $5 \times 10^{18} \text{ cm}^{-3}$ 、厚さ $0.5 \mu\text{m}$ で、その上に $0.5 \mu\text{m}$ のnドリフト層41bがある。両側のp<sup>+</sup>埋め込み領域42の間の間隔は、約 $5 \mu\text{m}$ である。n<sup>+</sup>ソース領域43の不純物濃度は $1 \times 10^{19} \text{ cm}^{-3}$ 、接合深さ $0.2 \mu\text{m}$ で、幅は約 $3 \mu\text{m}$ 、pゲート領域44のそれは、 $5 \times 10^{18} \text{ cm}^{-3}$ 、接合深さ $0.2 \mu\text{m}$ 、幅は約 $2 \mu\text{m}$ である。n<sup>+</sup>ソース領域43とpゲート領域44との間の間隔は約 $1 \mu\text{m}$ であり、nドリフト層41bが表面に達している。表面から掘り下げられた凹部47aの深さは、 $0.7 \mu\text{m}$ で、幅は約 $3 \mu\text{m}$ である。図の単位セルのピッチは約 $25 \mu\text{m}$ である。

【0031】図13の横型JFETと違っている点は、ソース電極47とドレイン電極48とが半導体基板の両面に設けられた縦型のFETとなっている点であるが、その動作は、基本的には図11のものと変わらない。すなわち、ゲート電極46に電圧を印加することによって、pゲート領域44から下方のチャネル領域50に空乏層が広がり、n<sup>+</sup>ソース領域43とnドリフト層41bとが電気的に絶縁される。その結果ドレイン電極38からソース電極37への電流が抑制される。図13に示したものと同一デプレッションタイプのJFETである。

【0032】図2(a)ないし(f)および図3(a)ないし(d)は、図1の実施例1のSiCJFETの製造方法を説明するための製造工程順の表面近傍の部分断面図である。以下順に説明する。まず、n<sup>+</sup>サブストレータ41a上に隣ドープのnドリフト層41bをエピタキシャル成長により積層した4H-SiC基板を準備する。例えば、nドリフト層41bの不純物濃度は $1 \times 10^{16} \text{ cm}^{-3}$ 、厚さは $10 \mu\text{m}$ である。そのnドリフト層41bの表面上に、多結晶シリコン膜1を減圧CVD法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクM1とする[図2(a)]。第一マスク

M1は、中央部のM1aと両側のM1bの各部分からなる。多結晶シリコン膜1の厚さは $1 \mu\text{m}$ とした。第一マスクM1は必ずしも多結晶シリコン膜である必要はなく、選択的なエッチングのマスクとなるものであれば、シリコンプロセスなどによく用いられる酸化けい素膜(以下SiO<sub>2</sub>膜と記す)、窒化けい素膜あるいはフォトレジストであってもよい。但し高温でイオン注入をする場合には、多結晶シリコンなどの高温に絶える材料を用いる必要がある。

【0033】多結晶シリコン膜1の第一マスクM1の上に熱CVD法によりSiO<sub>2</sub>膜2を堆積し、フォトリソグラフィでパターンを形成して、第二マスクM2とした後、これら第一、第二マスクM1、M2により規定された領域に、n型不純物となるイオン例えば窒素(以下Nと記す)イオン4aを注入する[同図(b)]。4bは注入されたN原子である。これはn<sup>+</sup>ソース領域43形成のためであり、加速電圧は $100 \text{ keV}$ 、ドーズ量は約 $5 \times 10^{15} \text{ cm}^{-2}$ である。イオン注入時の温度は、約 $800^\circ\text{C}$ である。高温でイオン注入することにより、活性化率を向上させることができる。第二マスクM2は、必ずしもSiO<sub>2</sub>膜である必要はないが、後の工程で第一マスクM1を残したまま除去することが必要であるため、第一マスクM1とは異なる材料とし、選択的なエッチングができるようにする必要がある。例えば、第一マスクM1として多結晶シリコン膜を使用した場合、第二マスクM2として、上の例のようにSiO<sub>2</sub>膜を用いれば、ふっ酸により第二マスク2だけを除去可能である。その逆も可能であり、その場合には四塩化炭素と酸素の混合ガス等を用いた反応性イオンエッチング(以下RIEと記す)により、SiO<sub>2</sub>膜と多結晶シリコン膜のエッチング速度を制御して多結晶シリコン膜のみをエッチングすることが可能である。このように、第一マスクM1に対して選択的な除去のできるものであればよい。第二のマスクM2は、端が第一マスクM1上にあれば良いのでマスク合わせは容易である。n型不純物としてはNの他に隣(以下Pと記す)などが用いられる。

【0034】SiO<sub>2</sub>膜の第二マスクM2を除去し、再度熱CVD法によりSiO<sub>2</sub>膜2を堆積し、フォトリソグラフィでパターンを形成して、第三マスクM3とした後、これら第一、第三マスクM1、M3で規定される領域に、p型不純物となるイオン例えばほう素(以下Bと記す)イオン5aを注入する[同図(c)]。5bは注入されたB原子である。これはpゲート領域44形成のためであり、加速電圧は $100 \text{ keV}$ 、ドーズ量は約 $5 \times 10^{15} \text{ cm}^{-2}$ である。この場合も第三マスクM3は必ずしもSiO<sub>2</sub>膜である必要はなく、後の工程で第一マスクM1に対して選択的な除去のできるものであればよい。第三マスクM3は、端が第一のマスクM1上にあれば良いのでマスク合わせは容易である。p型不純物となる不純物としてはBの他にアルミニウム(以下Alと記



す)などを用いることができる。

【0035】 $\text{SiO}_2$ 膜の第三マスクM3を除去し、フォトリソグラフィで第一マスクの一部M1bも除去し、第一マスクの一部M1aを残す[同図(d)]。残した第一マスクの一部M1aをマスクにして再びBイオン5aを注入する。[同図(e)]。これは $p^+$ 埋め込み領域42形成のためであり、加速電圧は400keV、ドーズ量は約 $1 \times 10^{15} \text{ cm}^{-2}$ である。加速電圧を高めたのは、深い不純物領域を形成するためである。 $p$ 型不純物としてはBの他にAlなどを用いてもよい。

【0036】残した第一マスクの一部M1aを除去し、全面にNイオン4aを注入する。[同図(f)]。4bは注入されたN原子である。これは $n$ チャネル領域50の濃度制御のためであり、加速電圧は200keV、ドーズ量は約 $1 \times 10^{12} \text{ cm}^{-2}$ である。この前に $p^+$ 埋め込み領域42のための深いイオン注入をおこなっているため、 $p^+$ 埋め込み領域42の上になる表面層の $n$ ドリフト層41bにはB原子が注入されている。Nイオンの注入により、表面層の抵抗を安定させることができる。熱処理後の表面層の不純物濃度は、約 $5 \times 10^{15} \text{ cm}^{-3}$ になる。

【0037】1600℃、2時間の熱処理をおこない、注入した不純物を活性化することによって $n^+$ ソース領域43、 $p$ ゲート領域44、 $p^+$ 埋め込み領域42の各領域が形成される[図3(a)]。先に述べたようにSiCでは不純物の拡散が殆ど起きないが、加速電圧の調節により、不純物領域の形成される深さを制御することができる。例えば、 $p^+$ 埋め込み領域42は、加速電圧を400keVと高くしたことによって、深さ0.8 $\mu\text{m}$ を中心にして、厚さ0.5 $\mu\text{m}$ の層ができており、その上には約0.5 $\mu\text{m}$ の $n$ ドリフト領域41bが残されている。 $p$ ゲート領域44、 $n^+$ ソース領域43の深さは、約0.2 $\mu\text{m}$ である。

【0038】表面に、CVD法により、 $\text{SiO}_2$ 膜2を堆積する[同図(b)]。フォトリソグラフィで第四マスクM4を形成し、四フッ化炭素( $\text{CF}_4$ )と酸素( $\text{O}_2$ )との混合ガスを用いたRIEで、 $n^+$ ソース領域43の表面から $p^+$ 埋め込み領域42に達する凹部47aを形成する[同図(c)]。フォトリソグラフィで $\text{SiO}_2$ 膜2にコンタクト用の開口を形成した後、アルミニウム合金膜を蒸着し、パターン形成して、ソース電極47およびゲート電極46とする。 $n^+$ サブストレーットの裏面にもドレイン電極を設けてプロセスを完了する[同図(d)]。

【0039】上記のような製造方法をとることにより、図1の高耐圧SiC縦型JFETとすることができた。実施例1のSiCJFETでは、第一マスクの一部M1bの端によって $n^+$ ソース領域43が規定され、第一マスクの一部M1bの別の端と、第一マスクの別の部分M1aとによって $p$ ゲート領域44が規定されている。さ

らに第一マスクの別の部分M1aによって、 $p^+$ 埋め込み領域42の端が規定されている。このように、不純物領域が第一マスクM1だけで規定されているため、それぞれが整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。第一マスクM1のパターン形成後に、各不純物領域の寸法が確認できるという利点もある。

【0040】チャネル領域の長さはMOSFETの特性を決定する主たるパラメータであることから、その制御は応用上極めて重要であるが、本実施例1のSiCJFETでは、実質的にチャネル長となるのは、 $p$ ゲート領域44の下部の $n$ チャネル領域50であり、チャネル長が短く均一に、精度よく形成され、安定した特性と高い歩留まりが得られる。試作した1500VクラスのJFETのオン抵抗は、 $15 \text{ m}\Omega \cdot \text{cm}^{-2}$ と低い値を示した。

【0041】また、 $p^+$ 埋め込み領域42を加速電圧の高いイオン注入で形成して、接合深さを深くしたため、容易に1500V以上の高耐圧が実現できた。 $n$ ドリフト層41bの表面層に不純物濃度制御のためのNイオン注入工程が加えられたことによって、MOSFETのしきい電圧を制御することができ、ノーマリオフのFETとすることもできる。

【0042】製造方法としては、幾つかの変形も考えられる。例えば、 $n^+$ ソース領域43と $p$ ゲート領域44とを形成するためのイオン注入の順序は逆でもよい。また、 $n$ チャネル領域50の不純物濃度制御のためのイオン注入は最初におこなってもよい。イオン注入を1000℃というような高温でなく、もっと低温でおこなうことにすれば、マスク材料の選択幅が広げられる。

【0043】[実施例2]図4は本発明第二の実施例にかかるSiCJFETの部分断面図である。これは図1の実施例1の変形例である。この例では、SiC基板表面に凹部が形成されず、 $n$ ドリフト層51bの表面層に $p^+$ 埋め込み領域52に達する $p^+$ コンタクト領域52aが形成されていて、その表面に $n^+$ ソース領域53と共通のソース電極57が設けられている。

【0044】 $n^+$ ソース領域53形成のためのNイオン注入の際の(図2(b)のM2に相当する)マスクとして、 $n^+$ ソース領域53の外側をも規定するマスクを使用し、更に別のマスクを用いて $p^+$ コンタクト領域52a形成のためのBイオン注入を行えば良い。このようにすれば、凹部を形成せず、基板表面に電極を設けることができる。

【0045】 $n^+$ ソース領域53の内側を規定するのは、第一マスクの一部(図2(b)のM1bに相当する)であることに代わりは無く、チャネル領域の長さは実施例1のSiCJFETと同様であり、 $p$ ゲート領域44の下部の $n$ チャネル領域60は、チャネル長が短く均一で、精度よく形成され、安定した特性と高い歩留まり



りが得られる。

【0046】〔実施例3〕図5は本発明第三の実施例にかかるSiC JFETの部分断面図である。これも図1のSiC JFETの変形ともいえる。図1のSiC JFETと違っている点は、ゲート電極66がpゲート領域64とnドリフト層61bの表面に共通に接触している点である。ここで、ゲート電極66は、SiC基板とショットキー接合を形成するような金属、例えばTi, Al, Ptなどを選択する。

【0047】実施例1のJFETでは図1からわかるように、pゲート領域44はゲート電極46が接触する部分でのみコンタクトが取られている。この接触抵抗を小さく抑えるためには、接触面積を大きくしなければならず、このコンタクト窓の大きさがチャネルの長さの最低値を制限していた。本実施例3のJFETはこの点を改良したものであり、ゲート電極66がpゲート領域64だけでなく、nドリフト層61bの表面にも接触しているため、コンタクト部分が広く取れ、チャネル領域を狭く設計することが可能となる。

【0048】この実施例3のJFETにおいても、n<sup>+</sup>ソース領域がpベース領域の表面層に自己整合して形成されており、実施例1のJFETと同様にチャネル長が、均一で精度よく形成され、安定した特性が歩留まりよく得られることは同じである。ただし、ゲート電極66は、SiC基板とショットキー接合を形成するような金属であり、ソース電極67と同じ金属とは限らない。或いは、ゲート電極66は、ショットキー接触をする金属とソース電極67と同じ金属との二層にしてもよい。これを製造するプロセスについてはほとんど図2、3とほぼ同一であり、説明を省く。

【0049】〔実施例4〕図6は本発明第四の実施例にかかるSiCMOSFETの部分断面図である。n<sup>+</sup>サブストレータ71a上にエピタキシャル成長によりnドリフト層71bが積層されたウェハにおいて、nドリフト層71bの表面から少し深い位置にp<sup>+</sup>埋め込み領域72が形成され、そのp<sup>+</sup>埋め込み領域72の上方のnドリフト層71bの表面層にn<sup>+</sup>ソース領域73が形成されている点は、これまでの例と同じであるが、pゲート領域はなく、p<sup>+</sup>埋め込み領域72の上方は、nチャネル領域80とされ、その表面上にMOS構造のゲート

【0050】すなわち、nドリフト層71bの表面上に、ゲート酸化膜75を介して多結晶シリコン層からなるゲート電極層76が設けられている。79はゲート電極層76と、ソース電極77とを絶縁するほう素燐シリカガラス(BPSG)の絶縁膜である。n<sup>+</sup>ソース領域73の表面から掘り下げられた凹部77aがあり、その表面に沿って、n<sup>+</sup>ソース領域73とp<sup>+</sup>埋め込み領域72との表面に共通に接触するソース電極77が設けられ、またn<sup>+</sup>サブストレータ71aの裏面に接触してド

レイン電極78が設けられている。主な各部のディメンションは、実施例1で述べた値とほぼ同じである。ゲート酸化膜75の厚さは50nm、ゲート電極層76の厚さは1μm、絶縁膜79の厚さは2μmである。

【0051】このMOSFETもACCUFETと呼ばれるものであり、ゲート電極層76に正電圧を印加することによって、ゲート電極層76直下のnドリフト層71bの表面部分に蓄積層が誘起され、ドレイン電極78と、ソース電極77との間に電流が流れる。また、ゲート電極層76に負電圧を印加すれば、ドレイン電極78とソース電極77との間の電流を遮断することができ、スイッチング機能を有す。ソース・ドレインの間の電圧はp<sup>+</sup>埋め込み領域72およびnドリフト層71bの間に印加されて大きな電圧を保持することが可能であり、高耐圧に適した構造になっている。

【0052】図7(a)ないし(e)および図8(a)ないし(d)は、図6の実施例4のSiCMOSFETの表面近傍の製造工程順の部分断面図である。以下順に工程について説明する。n<sup>+</sup>サブストレータ71a上に燐ドーブのnドリフト層71bをエピタキシャル成長により積層した4H-SiC基板を準備する。nドリフト層71bの不純物濃度、厚さ等は実施例1と同じでよい。そのnドリフト層71bの表面上に、多結晶シリコン膜を減圧CVD法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクM1とする〔図7(a)〕。第一マスクM1は、中央部のM1aと両側のM1bの各部分からなる。第一マスクM1は必ずしも多結晶シリコン膜である必要がないのは実施例1と同じである。

【0053】多結晶シリコン膜の第一マスクM1の上に熱CVD法によりSiO<sub>2</sub>膜を堆積し、フォトリソグラフィでパターンを形成して、第二マスクM2とした後、これら第一、第二マスクM1、M2により規定された領域に、n型不純物となるイオン例えばNイオン4aを注入する〔同図(b)〕。これはn<sup>+</sup>ソース領域73形成のためであり、加速電圧、ドーズ量等は実施例1と同じでよい。この第二マスクM2は、必ずしもSiO<sub>2</sub>である必要はないが、後の工程で第一マスクM1を残したまま除去することが必要であるため、第一マスクM1とは異なり、選択的なエッチングができる材料を選ぶ。第二マスクM2は、端が第一マスクM1上にあれば良いのでマスク合わせは容易である。n型不純物としてはNの他にPなどが用いられる。

【0054】SiO<sub>2</sub>膜の第二マスクM2を除去し、フォトリソグラフィで第一マスクの一部M1aを残した後、p型不純物となるイオン例えばBイオン5aを注入する〔同図(c)〕。これはp<sup>+</sup>埋め込み領域72形成のためであり、加速電圧は400keV、ドーズ量は約1×10<sup>15</sup>cm<sup>-2</sup>である。加速電圧を高めたのは、深い不純物領域を形成するためである。p型不純物はBの他

にAlなどが用いられる。

【0055】残した第一マスクの一部M1aを除去し、Nイオン4aを注入する。[同図(d)]。これはnチャネル領域80の不純物濃度制御のためであり、加速電圧は200keV、ドーズ量は約 $1 \times 10^{12} \text{ cm}^{-2}$ である。1600℃、2時間の熱処理をおこない、注入した不純物を活性化することによって、p<sup>+</sup>埋め込み領域72、n<sup>+</sup>ソース領域73、nチャネル領域80の各領域が形成される[同図(e)]。

【0056】表面に、1200℃、2時間の熱酸化によりゲート酸化膜75となるSiO<sub>2</sub>膜を形成し、続いて減圧CVD法によりゲート電極層となる多結晶シリコン膜1を約1μm堆積する[図8(a)]。ゲート酸化膜75は熱酸化で形成する他に、CVDにより成膜することも可能である。ゲート電極層76の材料としては多結晶シリコンの他にモリブデン(Mo)などが使用可能である。

【0057】フォトリソグラフィで多結晶シリコン膜1をパターン形成してゲート電極層76とした後、表面にCVD法により、ほう素燐シリカガラス(BPSG)などの絶縁膜79を堆積する[同図(b)]。フォトリソグラフィでパターンを形成し、四フッ化炭素(CF<sub>4</sub>)と酸素(O<sub>2</sub>)との混合ガスを用いたRIEで、n<sup>+</sup>ソース領域73の表面からp<sup>+</sup>埋め込み領域72に達する凹部77aを形成する[同図(c)]。

【0058】フォトリソグラフィで絶縁膜79にコンタクト用の開口を形成した後、アルミニウム合金を蒸着し、パターン形成して、ソース電極77および図示しないゲート電極とする。n<sup>+</sup>サブストレーットの裏面にもドレイン電極を設けてプロセスを完了する[同図(d)]。この実施例4のMOSFETにおいても、第一マスクの一部M1bの端によってn<sup>+</sup>ソース領域73が規定され、第一マスクの別の部分M1aによって、p<sup>+</sup>埋め込み領域72の端が規定されている。このように、不純物領域が第一マスクM1だけで規定されているため、それぞれが整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。

【0059】従って、実施例1のJFETと同様に1.5μm程度のチャネル長が、均一で精度よく実現され、安定した特性が歩留まりよく得られる。第一マスク1の形成後に、各不純物領域の寸法が確認できるという利点もある。nドリフト層71bの表面層に不純物濃度制御のためのNイオン注入工程が加えられてnチャネル領域80とされていることによって、MOSFETのしきい電圧を制御することができ、特に、ノーマリオフのFETとすることもできる。

【0060】また、ゲート酸化膜75がSiC基板上に平面状に形成されているので、従来のトレンチタイプのMOSFETで見られたゲート酸化膜のコーナー部にお

ける電界のストレスの問題が無く、高耐圧化が可能である。製造方法としては、幾つかの変形も考えられる。例えば、nチャネル領域80の不純物濃度制御のためのイオン注入は最初におこなってもよいし、第二マスクM2と第三マスクM3との形成は逆の順でも良い。

【0061】n<sup>+</sup>ソース領域73形成のためのNイオン注入の際に、n<sup>+</sup>ソース領域73の外側を規定するマスクを使用し、更に別のマスクを用いてp<sup>+</sup>コンタクト領域52a形成のためのBイオン注入を行えば、凹部77aを形成せず、基板表面に電極を設けることができる。その場合もチャネル領域の長さは実施例4のSiCMOSFETと同様に、均一に、精度よく形成され、安定した特性と高い歩留まりが得られる。

【0062】[実施例5]図9は本発明第五の実施例にかかるSiCMOSFETの部分断面図である。n<sup>+</sup>サブストレーット81a上にエピタキシャル成長により堆積したnドリフト層81bの表面から少し深い位置にp<sup>+</sup>埋め込み領域82が形成され、p<sup>+</sup>埋め込み領域82の上方のnドリフト層81bの表面層にpベース領域82が形成され、その上方には選択的にn<sup>+</sup>ソース領域83が形成されている。そしてpベース領域82の端の部分は、n<sup>+</sup>ソース領域83から遠ざかる程、ほぼ直線的に接合深さが浅くなっているのが特徴的である。また、pベース領域82と一部重複するように、pベース領域82より深い部分にp<sup>+</sup>コンタクト領域82aが形成されている。n<sup>+</sup>ソース領域83が形成されていない部分のpベース領域82の上方は、nチャネル領域90とされ、その上には図6のMOSFETと同様のMOS構造のゲートが設けられている。すなわち、ゲート酸化膜85を介して多結晶シリコン層からなるゲート電極層86が設けられている。89はゲート電極層と、ソース電極87とを絶縁するBPSGの絶縁膜である。n<sup>+</sup>ソース領域83の表面から掘り下げられた凹部87aがあり、n<sup>+</sup>ソース領域83とp<sup>+</sup>コンタクト領域82との表面に共通に接触してソース電極87が設けられ、またn<sup>+</sup>サブストレーット81aの裏面に接触してドレイン電極88が設けられている。

【0063】主なディメンジョンの一例は、次のような値である。n<sup>+</sup>サブストレーット41aの不純物濃度は $1 \times 10^{18} \text{ cm}^{-3}$ 、厚さ350μm、nドリフト層41bのそれは、 $1 \times 10^{16} \text{ cm}^{-3}$ 、厚さ10μm。pベース領域82の最高不純物濃度は $5 \times 10^{16} \text{ cm}^{-3}$ 、接合深さ1.5μm、両側のpベース領域82の間の間隔は、約6μmである。n<sup>+</sup>ソース領域43の不純物濃度は $1 \times 10^{19} \text{ cm}^{-3}$ 、接合深さ0.2μmで、幅は約5μm、p<sup>+</sup>コンタクト領域82の最高不純物濃度は $1 \times 10^{19} \text{ cm}^{-3}$ 、接合深さ2.0μm、幅は約5μm、nチャネル領域90の不純物濃度は $5 \times 10^{15} \text{ cm}^{-3}$ 、接合深さ0.5μmである。n<sup>+</sup>ソース領域83の端とpベース領域82の端との間の間隔は約2μmである。表面

から掘り下げられた凹部87aの深さは、 $0.7\mu\text{m}$ で、幅は約 $3\mu\text{m}$ である。図の単位セルのピッチは約 $30\mu\text{m}$ である。ゲート酸化膜85の厚さは $50\text{nm}$ 、ゲート電極層86の厚さは $1\mu\text{m}$ 、絶縁膜89の厚さは $2\mu\text{m}$ である。

【0064】図10(a)ないし(e)および図11(a)ないし(e)は、図9の実施例5のSiCMOSFETの表面近傍の製造工程順の部分断面図である。以下順に工程について説明する。まず、 $n^+$ サブストレート上に燐ドープのnドリフト層81bをエピタキシャル成長により積層した4H-SiC基板を準備する。nドリフト層81bの表面上に、多結晶シリコン膜を減圧CVD法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクM1とする。

【0065】特にこのパターニングの際、第一マスクM1の端部に $1\sim 2\mu\text{m}$ にわたりテーパ部8を形成することが重要である。これは、次のpベース領域形成のためのイオン注入においてチャネル長が第一マスクM1のテーパ部8の角度で制御されるからである。従って、このテーパ角度は所定の設計に倣って決められなければならない。そしてこの角度は、第一マスク1の薄膜をプラズマエッチング等によりエッチングする際のエッチング条件を選ぶことによって制御可能である。或いは、薄膜の上部にイオン注入するなどしてダメージを与えておき、表面近傍のみをエッチングされやすくしておく、ゆるやかなテーパが得られる。その際のイオン注入のドーズ量を制御することにより、テーパ角を制御する方法もある。

【0066】その第一マスクM1をマスクとしてp型不純物となるイオン例えばほう素(B)イオン5aを注入する[図10(a)]。5bは注入されたB原子である。これはpベース領域82形成のためであり、加速電圧は $300\text{keV}$ 、ドーズ量は約 $1\times 10^{15}\text{cm}^{-2}$ である。加速電圧を高めたのは、深い不純物領域を形成するためである。第一マスクM1の無い領域では不純物は深く注入され、第一マスクM1が厚さが増すに従ってほぼ直線的に次第に浅くなって、不純物原子は図のような分布をする。第一マスクM1の厚さをある程度薄くしておけば、不純物注入領域は表面にまで達せず、埋め込み型の領域とすることができる。p型不純物はBの他にAlなどが用いられる。第一マスクM1は必ずしも多結晶シリコン膜である必要はないのは実施例1と同じである。

【0067】次に同じ第一マスクM1をマスクとしてn型不純物となるイオン例えばNイオン4aを注入する[同図(b)]。4bは注入されたn原子である。これは $n^+$ ソース領域83形成のためであり、加速電圧等は実施例1と同じ $100\text{keV}$ 、ドーズ量は約 $5\times 10^{15}\text{cm}^{-2}$ でよい。この場合も、第一マスクM1の無い領域では不純物は深く注入され、第一マスクM1が厚くなると次第に浅くなって、不純物原子は図のような分布をす

る。但し、加速電圧を低くしているので、注入される領域がBイオンの注入領域と異なる。テーパ部8の角度が同じであれば、p型不純物の注入領域とn型不純物の注入領域との間隔は一定になる。

【0068】多結晶シリコン膜の第一マスクM1の上に熱CVD法により $\text{SiO}_2$ 膜2を堆積する[同図(c)]。

RIEで全面エッチングすることにより、第一マスクM1のテーパ部8の側方にサイドウォール9を形成した後、これら第一マスクM1およびサイドウォール9により規定された領域に、p型不純物となるイオン例えばBイオン5aを注入する[同図(d)]。これは高濃度の $p^+$ コンタクト領域84形成のためであり、加速電圧、 $400\text{keV}$ 、ドーズ量は約 $1\times 10^{15}\text{cm}^{-2}$ である。p型不純物としてはBの他にAlなどが用いられる。

【0069】第一マスクM1、サイドウォール9を除去した後、全面にNイオン4aを注入をする。[同図(e)]。これはnチャネル領域90の不純物濃度制御のためであり、加速電圧は $200\text{keV}$ 、ドーズ量は約 $1\times 10^{12}\text{cm}^{-2}$ である。これにより、例えばしきい値が制御できる。 $1600^\circ\text{C}$ 、2時間の熱処理をおこなひ、注入した不純物を活性化することによって各領域が形成される[図11(a)]。このようにして、pベース領域82、 $n^+$ ソース領域83とをずらして形成することができる。

【0070】表面に、 $1200^\circ\text{C}$ 、2時間の熱酸化によりゲート酸化膜85となる厚さ $50\text{nm}$ の熱 $\text{SiO}_2$ 膜6を形成し、続いて減圧CVD法により多結晶シリコン膜1を約 $1\mu\text{m}$ 堆積する[同図(b)]。ゲート酸化膜85は熱酸化で形成する他に、CVDにより成膜することも可能である。フォトレジストを塗布し、フォトリソグラフィで多結晶シリコン膜1をパターン形成してゲート電極層86とした後、表面にCVD法により、ほう素燐シリカガラス(BPSG)などの絶縁膜89を堆積し、フォトリソグラフィでパターンを形成する[同図(c)]。

【0071】四フッ化炭素( $\text{CF}_4$ )と酸素( $\text{O}_2$ )との混合ガスを用いたRIEで、 $n^+$ ソース領域83の表面から $p^+$ コンタクト領域82aに達する凹部87aを形成する[同図(d)]。フォトリソグラフィで絶縁膜89にコンタクト用の開口を形成した後、アルミニウム合金を蒸着し、パターン形成して、ソース電極87および図示しないゲート電極とする[同図(e)]。 $n^+$ サブストレートの裏面にもドレイン電極を設けてプロセスを完了する。

【0072】この実施例5のMOSFETにおいては、第一マスク1の端部をテーパ状とし、p型不純物とn型不純物の注入の際の加速電圧を変えることによって、 $n^+$ ソース領域83とpベース領域82の端が規定されている。すなわち両者の間の間隔であるチャネル長は第



ーマスクM1のテーパ部8で規定される。このように、不純物領域が第一マスクだけで規定されているため、両者が整合しており、位置ずれ等のマスク合わせによる不均一の問題が起きない。

【0073】従って、チャネル長が均一に精度よく形成され、安定した特性が歩留まりよく得られる。また、第一マスクM1のテーパ部8の角度を変えれば、両者の間隔すなわちチャネル領域の長さは自由に制御できることになり、オン抵抗と耐圧のバランスも取りやすい。第一マスク1の形成後に、各不純物領域の寸法が確認できるという利点もある。

【0074】nドリフト層81bの表面層に不純物濃度制御のためのNイオン注入工程が加えられたことによって、MOSFETのしきい電圧を制御することができ、特に、ノーマリオフのFETとすることもできる。製造方法としては、幾つかの変形も考えられる。例えば、nチャネル領域90の不純物濃度制御のためのイオン注入は最初におこなってもよい。また、pベース領域82のためのBイオンの注入とn<sup>+</sup>ソース領域83形成のためのNイオンの注入の順は逆でもよい。最初にサイドウォール領域を形成し、p<sup>+</sup>コンタクト領域84形成のためのイオン注入をおこなっても良い。

【0075】この例でもゲート酸化膜85がSiC基板上に平面状に形成されているので、従来のトレンチタイプのMOSFETで見られたゲート酸化膜コーナー部における電界のストレスの問題が無く、高耐圧化が可能である。また、この実施例では、p<sup>+</sup>コンタクト領域82aを埋め込み型の領域としたが、n<sup>+</sup>ソース領域83形成のためのNイオン注入の際に、n<sup>+</sup>ソース領域83の外側を規定するマスクを使用し、p<sup>+</sup>コンタクト領域82aを多重注入により表面にまで達するようにすれば、基板表面にソース電極87を設けることができ、凹部87aを形成する必要が無い。

【0076】[実施例6] 図12(a)ないし(e)は、図9のSiCMOSFETとほぼ同じSiCMOSFETの別の製造方法を説明するための製造工程順の表面近傍の部分断面図である。以下順に工程について説明する。まず、n<sup>+</sup>サブストレート上に隣ドープのnドリフト層91bをエピタキシャル成長により積層した4H-SiC基板を準備する。nドリフト層91bの不純物濃度、厚さ等は実施例1と同じでよい。そのnドリフト層91bの表面上に、プラズマCVD法により厚さ約2μmのSiO<sub>2</sub>膜2を堆積し、フォトリソグラフィでパターンを形成して、第三マスクM3とする。

【0077】その第三マスクM3をマスクとしてp型不純物となるイオン例えばBイオン5aを注入する[図12(a)]。5bは注入されたB原子である。これは高濃度のp<sup>+</sup>コンタクト領域94形成のためであり、加速電圧、400keV、ドーズ量は約 $1 \times 10^{15} \text{ cm}^{-2}$ である。p型不純物としてはBの他にAlなどが用いられ

る。

【0078】次に、CF<sub>4</sub>+H<sub>2</sub>ガスを用いたプラズマエッチングにより、第三マスクM3をエッチバックして、端を1~2μmにわたりテーパ状にした第一マスクM1とする[同図(b)]。このとき、全体の厚さも薄くなり、厚さは約1μmになる。これは、実施例5のSiCMOSFETの時と同様に、次のpベース領域形成のためのイオン注入においてチャネルが第一マスクの端部のテーパ角度で制御されるようにするものである。

【0079】その端部をテーパ状にした第一マスクM1をマスクとしてp型不純物となるイオン例えばBイオン5aを注入する[同図(c)]。これはpベース領域92形成のためであり、加速電圧は300keV、ドーズ量は約 $1 \times 10^{15} \text{ cm}^{-2}$ である。第一マスクM1の無い領域では不純物は深く注入され、第一マスクM1が厚さが増すに従って次第に浅くなって、不純物原子は図のような分布をする。

【0080】次に同じ端部をテーパ状にした第一マスクM1をマスクとしてn型不純物となるイオン例えばNイオン4aを注入する[同図(d)]。これはn<sup>+</sup>ソース領域93形成のためであり、加速電圧は100keV、ドーズ量は約 $5 \times 10^{15} \text{ cm}^{-2}$ である。加速電圧を低くしているの、注入される領域がp型不純物の注入領域と異なっている。

【0081】第一マスクM1を除去した後、全面にNイオン4aを注入をする。[同図(e)]。これはnドリフト層91bの表面層のnチャネル領域の不純物濃度制御のためであり、加速電圧は200keV、ドーズ量は約 $1 \times 10^{12} \text{ cm}^{-2}$ である。これにより、例えばしきい値が制御できる。これ以降は、図10(a)以降の注入した不純物の活性化、電極の形成等をおこなう。

【0082】この方法を取れば、第三マスクM3をバックエッチして第一マスクM1としたので、マスク材料を改めて形成する必要がない。そして、テーパ部の角度も均一になって、pベース領域92とnソース領域93との間隔が規定されるため、両者が整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。そして、チャネル長が均一に精度よく形成され、安定した特性が歩留まりよく得られる。

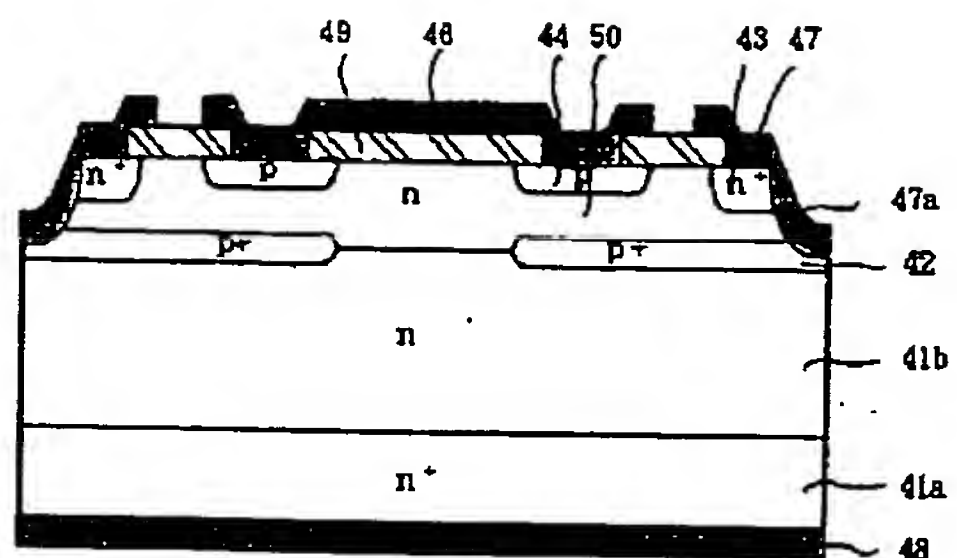
【0083】製造方法としては、幾つかの変形も考えられる。例えばpベース領域形成のためのp型不純物イオンの注入[図12(c)]と、nソース領域形成のためのn型不純物イオンの注入[図12(d)]とは逆の順序でもよく、nチャネル領域の不純物濃度制御のためのイオン注入[図12(e)]は最初におこなってもよい。

【0084】

【発明の効果】以上説明したように本発明によれば、炭化けい素縦型FETの製造方法において、第一のマスクと一部重複する第二のマスクとを用いて第一のマスクの

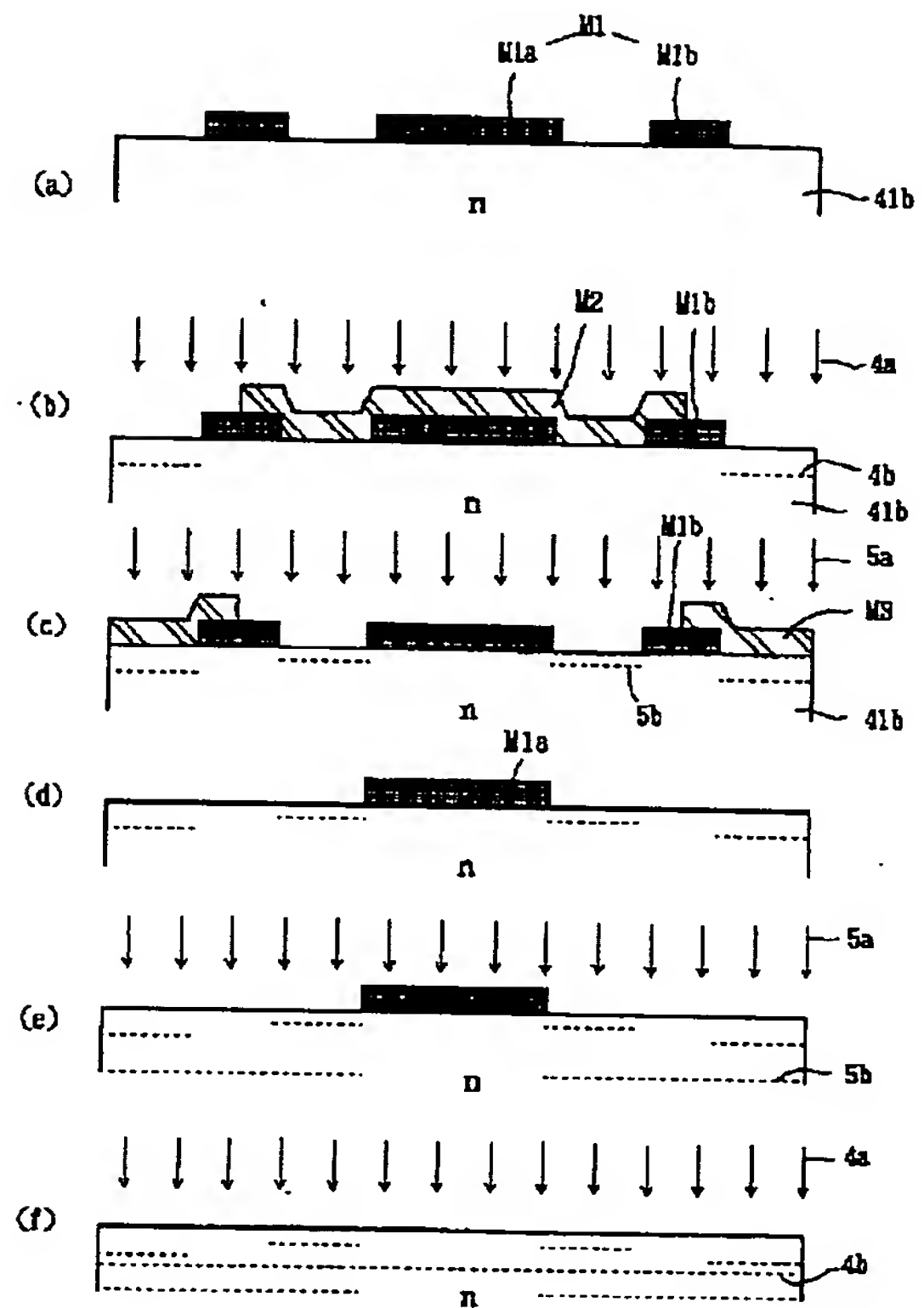


【図 1】

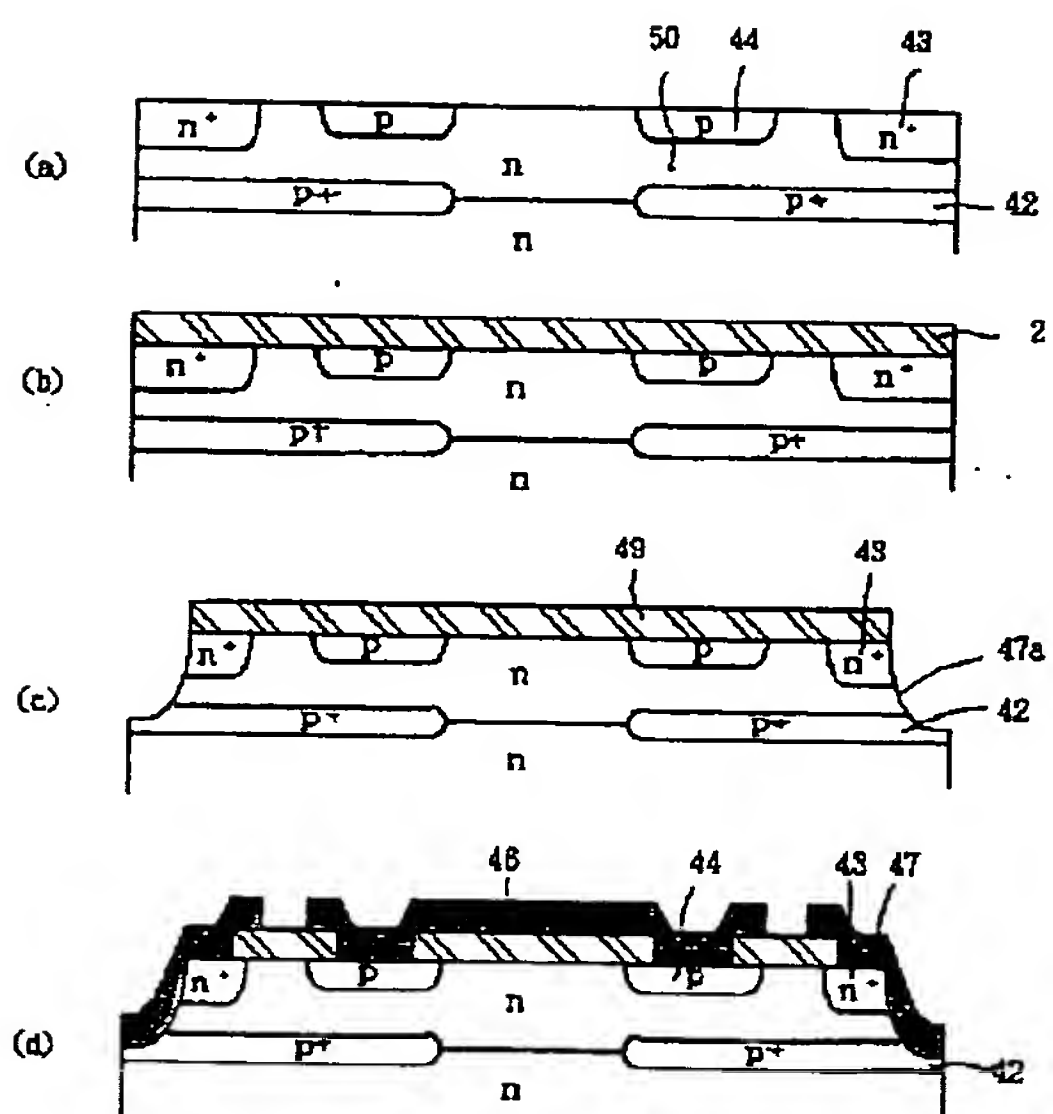


- |                          |             |
|--------------------------|-------------|
| 41a n <sup>+</sup> ドレイン層 | 47 ソース電極    |
| 41b n ドリフト層              | 47a 凹部      |
| 42 p <sup>+</sup> 埋め込み領域 | 48 ドレイン電極   |
| 43 n <sup>+</sup> ソース領域  | 49 絶縁膜      |
| 44 p ゲート領域               | 50 n チャネル領域 |
| 48 ゲート電極                 |             |

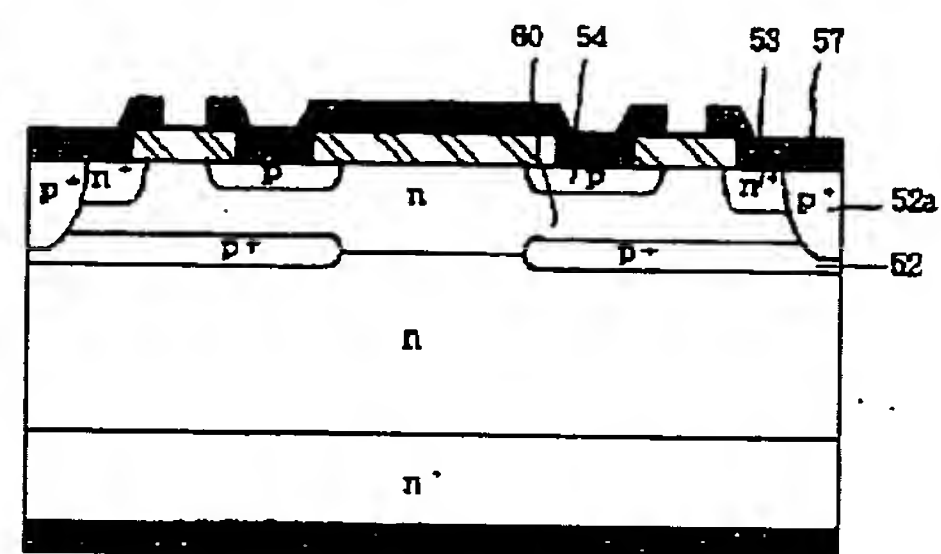
【図 2】



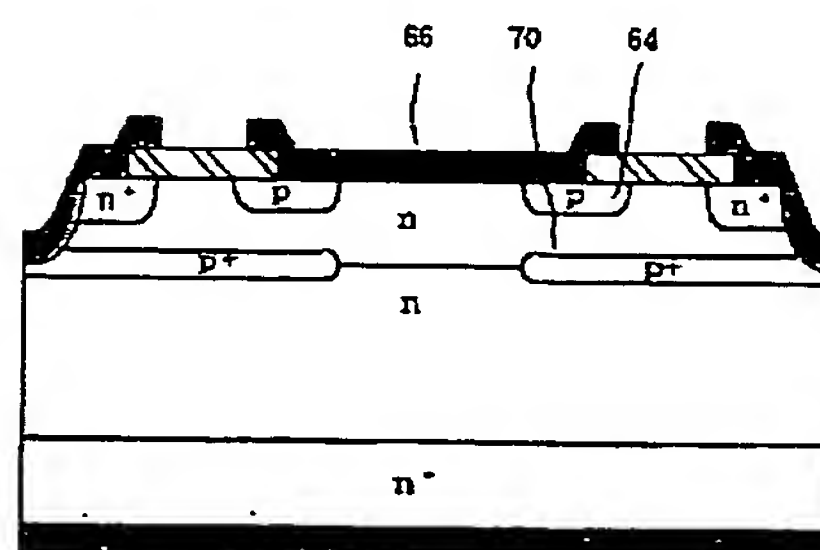
【図 3】



【図 4】

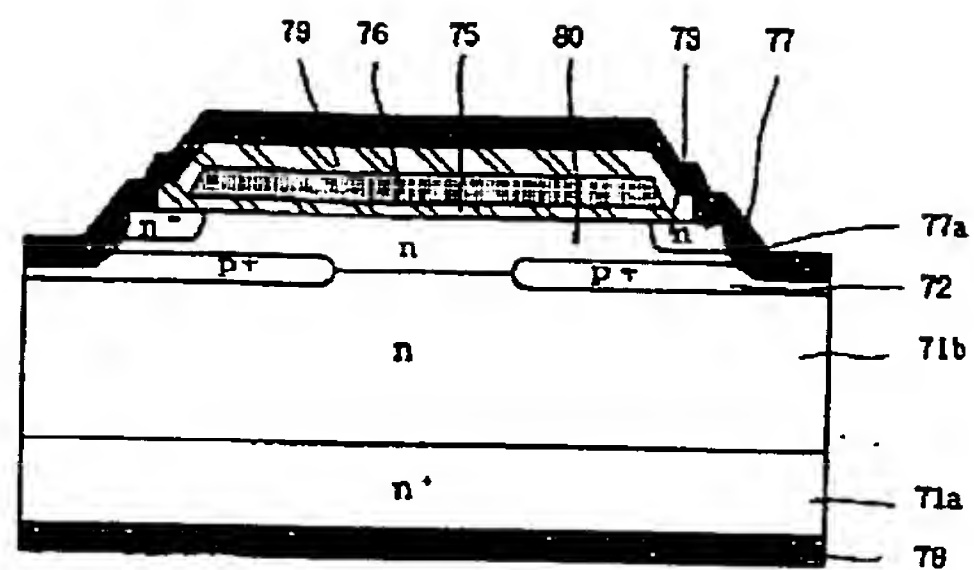


【図 5】

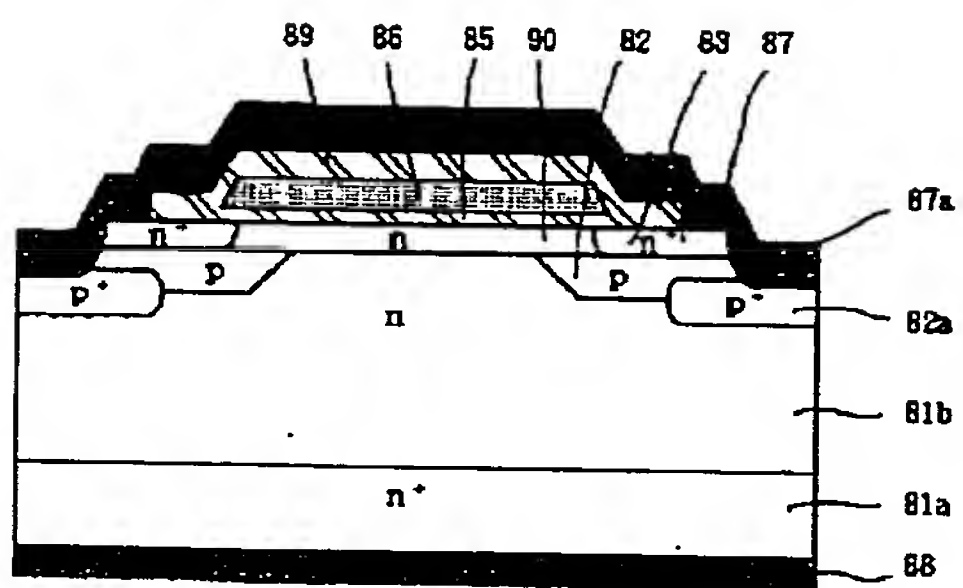




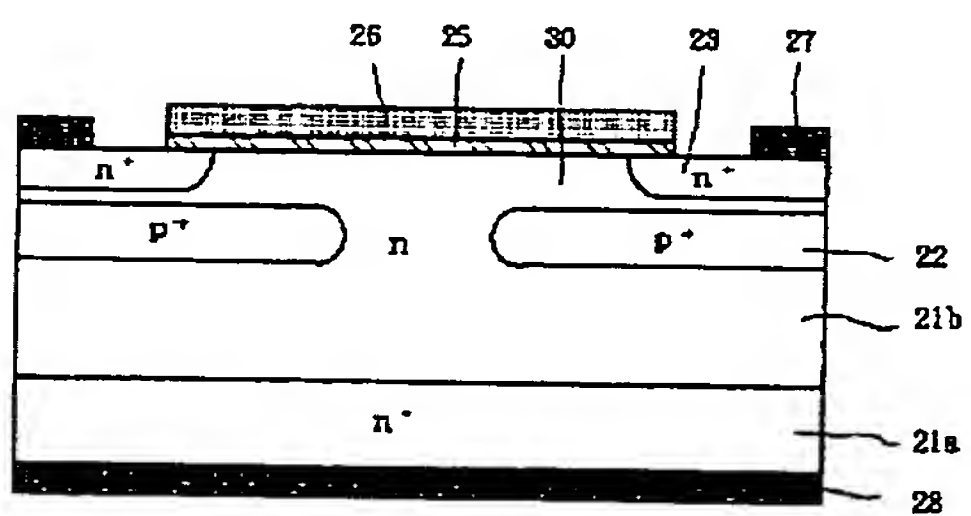
【図6】



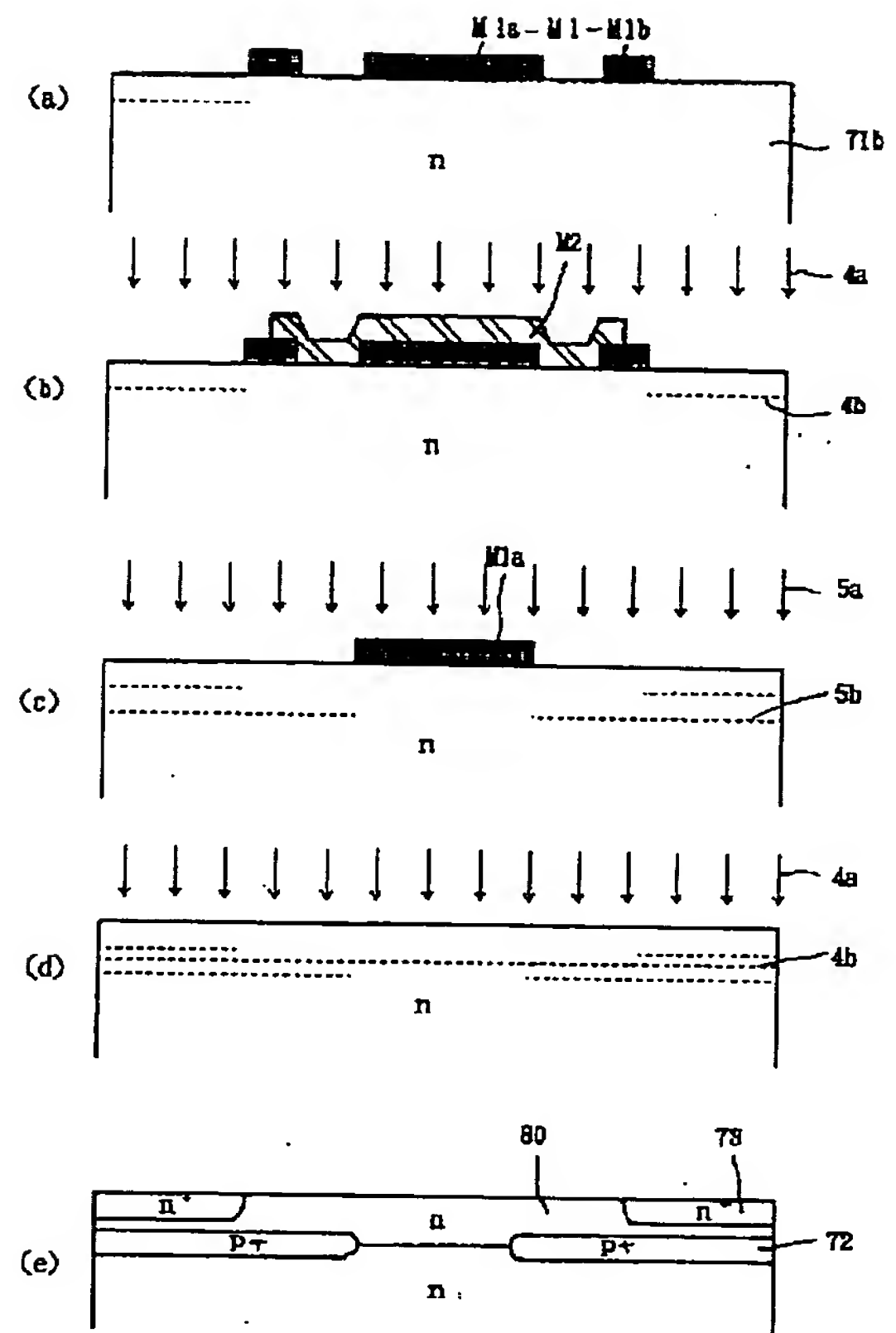
【図9】



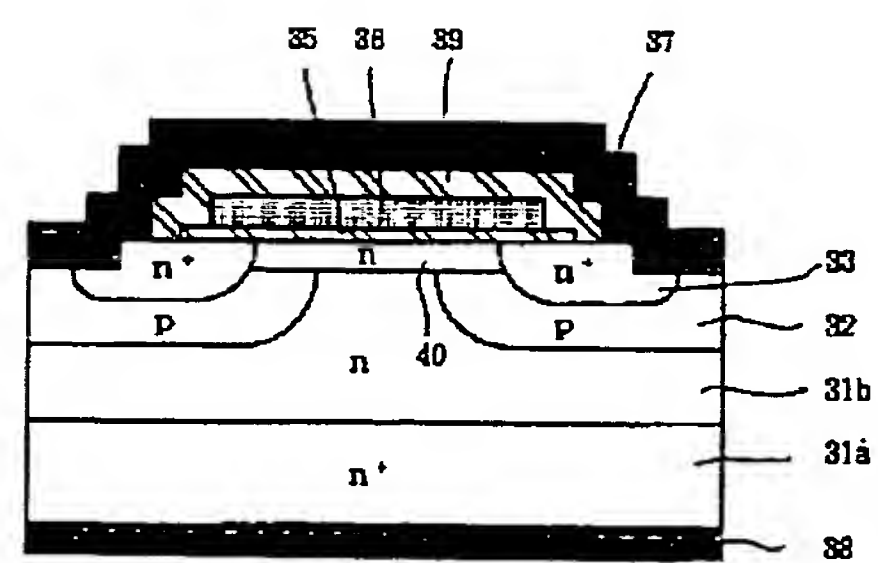
【図14】



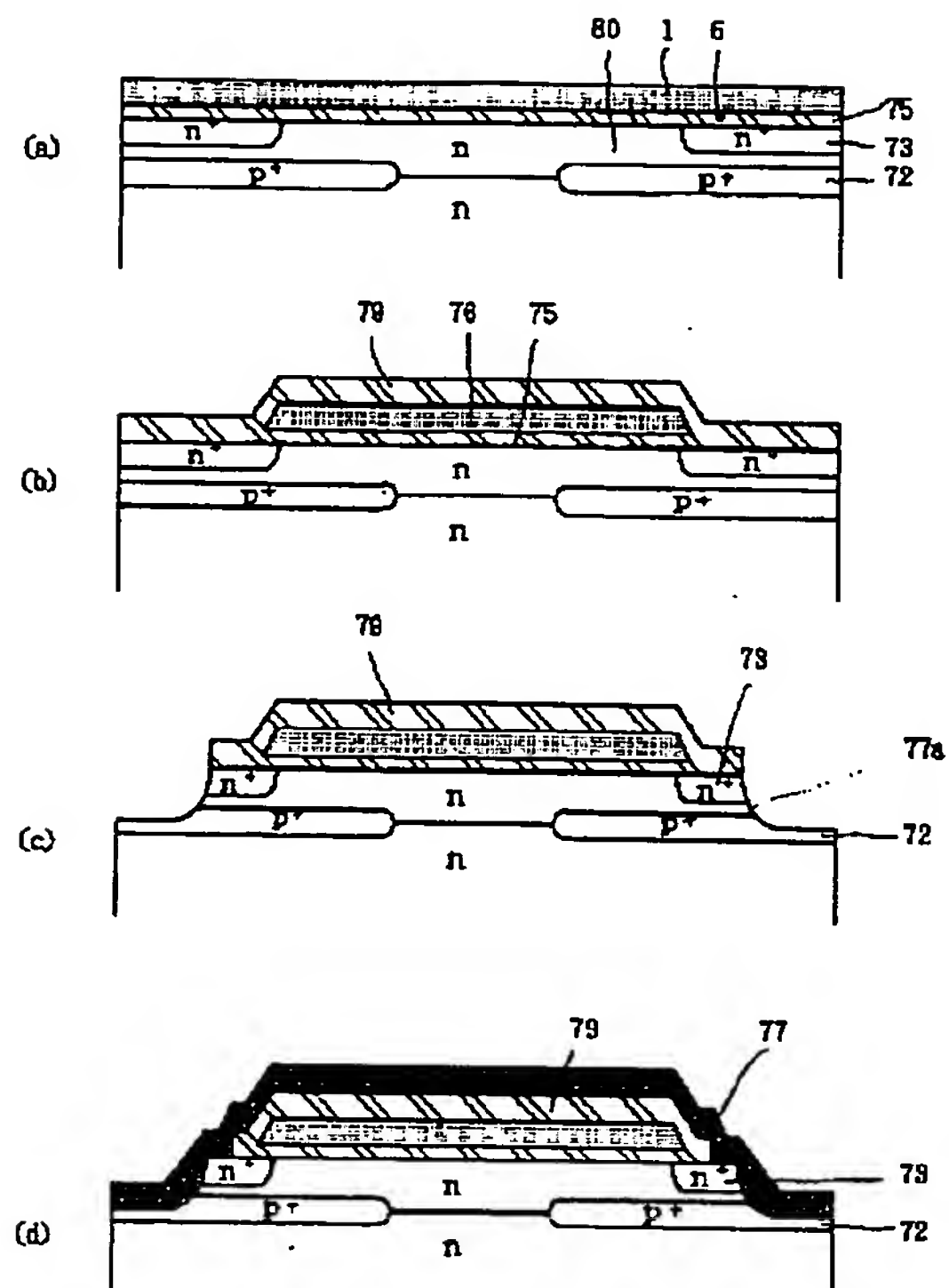
【図7】



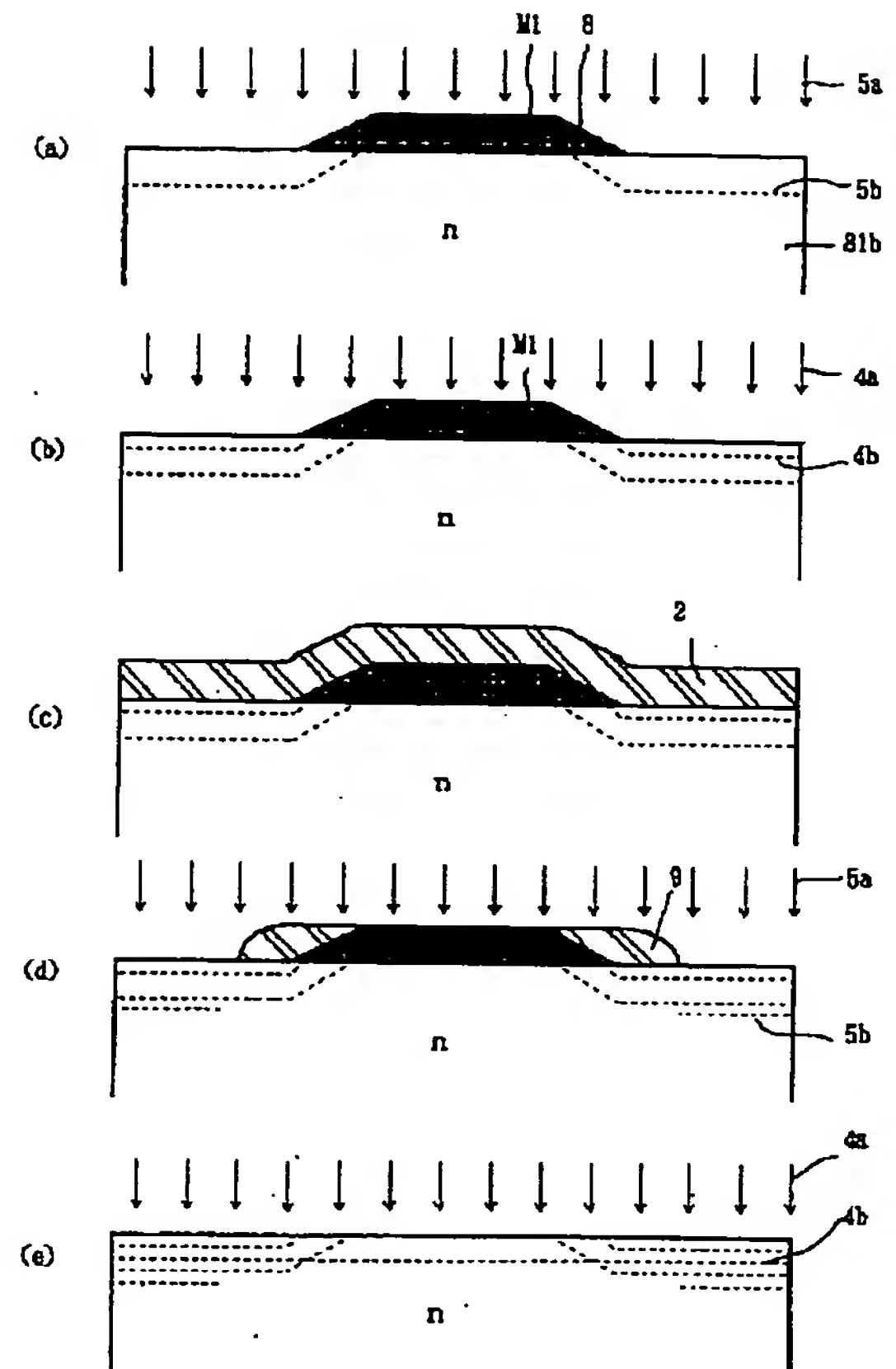
【図15】



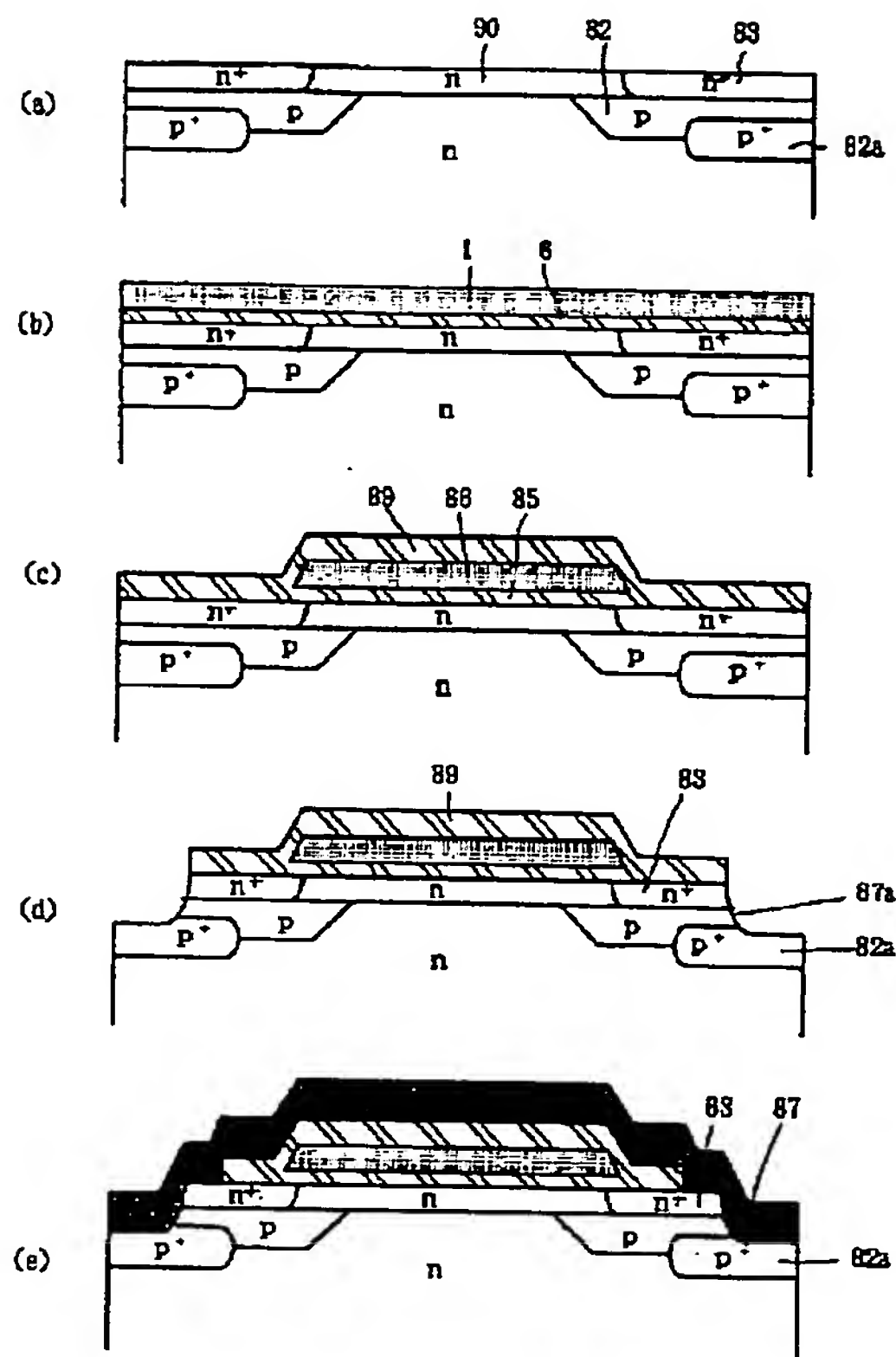
【図 8】



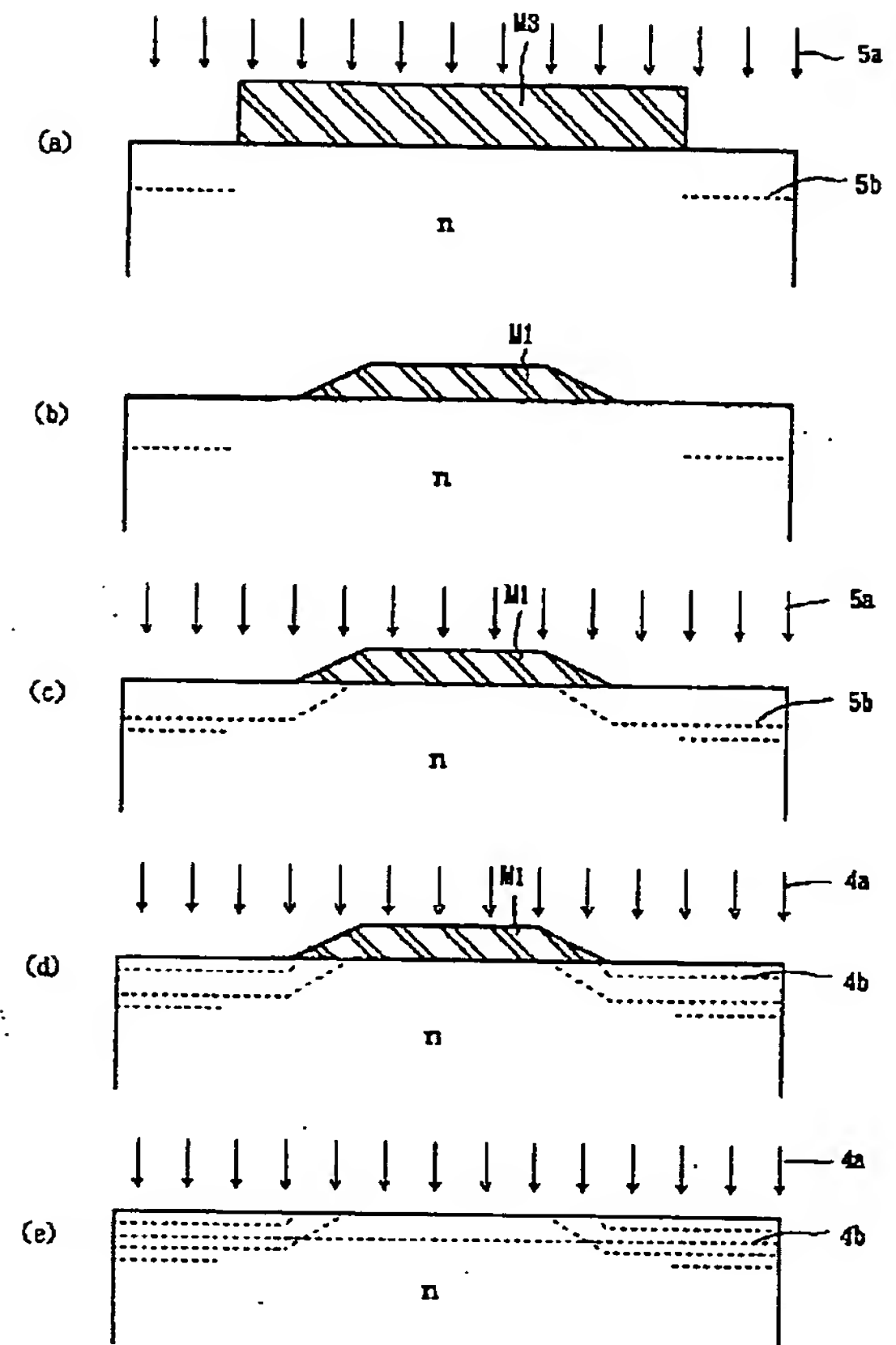
【図 10】



【図11】



【図12】





**\* NOTICES \***

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

**CLAIMS**

---

[Claim(s)]

[Claim 1] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate Some of one [ of the first mask ] edges prescribe one edge of the first conductivity-type source field. The manufacture approach of the silicon carbide end-fire array FET characterized by for some other ends of the first mask and other parts of the first mask prescribing the second conductivity-type gate field, and for other parts of said first mask prescribing the edge of the second conductivity-type embedding field, and forming each field.

[Claim 2] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, The manufacture approach of the silicon carbide end-fire array FET which consists of the process which forms the fifth mask which

consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[Claim 3] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The process which forms the fourth mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type embedding field with the mask, The manufacture approach of the silicon carbide end-fire array FET which consists of the heat treatment process for activating the introduced impurity, the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[Claim 4] The manufacture approach of the silicon carbide end-fire array FET according to claim 2 or 3 characterized by performing each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation by the ion implantation.

[Claim 5] The manufacture approach of the silicon carbide end-fire array FET according to claim 1 to 4 characterized by preparing the electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer.

[Claim 6] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate The manufacture approach of the silicon carbide end-fire array FET characterized by specifying one edge of the first conductivity-type source field with a part of first mask, and specifying the edge of the second conductivity-type embedding field by other parts of said first mask.

[Claim 7] The process at which the first conductivity-type drift layer which consists of silicon

carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, The gate electrode which serves as a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 8] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type embedding field with the mask, The heat treatment process for activating the introduced impurity, and the process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which covers an insulator layer, and the process which prepares the aperture for contact in the insulator layer, and vapor-deposits a metal membrane, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the gate electrode which consists of the metal membrane and contacts a polycrystalline silicon layer, the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 9] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-



type drift layer, The second conductivity-type base region alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate The manufacture approach of the silicon carbide end-fire array FET characterized by for a part with the thick thickness of the first mask of the shape of a taper with a loose edge prescribing one edge of the first conductivity-type source field, and specifying the edge of the second conductivity-type base region by the part with the thin thickness of the first mask of said first mask.

[Claim 10] The substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth is used. The process which forms the first mask of the shape of a taper with a loose edge on the front face of the first conductivity-type drift layer, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thin thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The heat treatment process for activating the introduced impurity, and the process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The gate electrode which serves as a process which prepares the aperture for contact and vapor-deposits a metal membrane after covering an insulator layer from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 11] The substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth is used. The process which forms the first mask of the shape of a taper with a loose edge on the front face of the first conductivity-type drift layer, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process

which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field with the mask, The gate electrode which serves as a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 12] The manufacture approach of the silicon carbide end-fire array FET according to claim 10 or 11 characterized by preparing a sidewall in the side of the first mask and using the first mask and its sidewall as the third mask.

[Claim 13] The manufacture approach of the silicon carbide end-fire array FET according to claim 9 to 11 characterized by carrying out etchback of the third mask, and an edge considering as the first mask of the shape of a loose taper after passing through the process which forms the third mask with the thick thickness for the second conductivity-type contact field formation which arrives at the second conductivity-type base region, and the process which introduces an impurity with the mask previously.

[Claim 14] The manufacture approach of the silicon carbide end-fire array FET according to claim 6 to 13 characterized by performing each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation by the ion implantation.

[Claim 15] The manufacture approach of the silicon carbide end-fire array FET according to claim 1 to 14 characterized by adding the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer.

[Claim 16] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, In the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate Silicon carbide end-fire array FET characterized by becoming shallow almost linearly, so that the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field.

[Claim 17] Silicon carbide end-fire array FET according to claim 16 characterized by preparing the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region, and a source electrode touching the front face of the second conductivity-type contact field with high high impurity concentration from the second conductivity-type base region so that a part may overlap the second conductivity-type base region.

[Claim 18] Silicon carbide end-fire array FET according to claim 16 characterized by embedding the second conductivity-type contact field, being prepared, preparing the crevice which arrives at

the second conductivity-type contact field from the front face of the first conductivity-type source field, and a source electrode touching the exposure front face of the second conductivity-type contact field.

[Claim 19] Silicon carbide end-fire array FET according to claim 16 to 18 to which high impurity concentration of a channel field is characterized by being high concentration from that of the first conductivity-type drift layer.

---

[Translation done.]



**\* NOTICES \***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

## DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the manufacture approach of a vertical mold field-effect transistor (it is described as Following FET) and the vertical mold electric field effect FET with the gate of the assembling die which used silicon carbide as a semiconductor material and which is a power semiconductor device, or the MOS mold of metal-oxide film-semiconductor structure.

[0002]

[Description of the Prior Art] Since a band gap is large and the maximum insulation electric field are large a figure single [ about ] as compared with silicon (it is described as Following Si), silicon carbide (it is described as Following SiC) is an ingredient with which the application to a next-generation power semiconductor device is expected. It is applied to various electron devices until now using the single crystal wafer called 4 H-SiC or 6 H-SiC, and it is thought that it is especially suitable for an elevated temperature and the component for large power. The above-mentioned crystal is the alpha phase SiC of the form which carried out the laminating of a sphalerite mold and the wurtzite mold. The semiconductor device is made also for the crystal of the beta phase SiC otherwise called 3 C-SiC as an experiment. [ , for example, Weitzel, by which CMOS-IC which is the general-purpose semiconductor devices, such as schottky diode, end-fire array MOSFET, and a thyristor, as a component for power is recently made as an experiment, and it is checked from the property as compared with the conventional Si semiconductor device that a property is very good, :IEEE Trans.on Electron Devices besides C.W., and vol. -- 43, No.10, and pp.1732-1741 --] (1997) . Some examples of MOSFET are shown below.

[0003] Drawing 13 is the fragmentary sectional view of the unit cell of junction type FET (it omits Following JFET) currently developed as one of the RF components [ and Abstracta of Int.Conf.on Silicon Carbide besides Sheppard and S.T., III-Nitrides and Related Materials] (1997). p+ It is n+ to the surface layer of n drift layer 11 by which the laminating was carried out on the substrate 10. The source field 13, p gate field 15, and n+ The drain field is formed. n+ The source field 13 and n+ The drain field 14 and p gate field 15 are contacted, and the source electrode 17, the drain electrode 18, and the gate electrode 16 are formed, respectively.

[0004] When an electrical potential difference is impressed to the gate electrode 16 with this structure, they are p gate field 15 to p gate field 15, and p+. A depletion layer spreads to the n channel field 20 between substrates 10. The current between the source electrode 17 and the drain electrode 18 is controlled by this. Moreover, a current flows again between the drain electrode 18 and the source electrode 17 by removing the electrical potential difference impressed to the gate electrode 16. Thus, the current between source drains serves as a component switchable [ with gate voltage ]. Since this JFET depletion-izes a channel field by

electrical-potential-difference impression to the gate electrode 16, it is called a depletion type. A front face to p+ The slot which reaches a substrate 10 is formed and it fills up with the insulator layer 19 because [ of isolation ].

[0005] On the other hand, drawing 14 is one sort of a vertical mold MOSFET [Shenoy, J.N. others, Abstracts of Int.Conf.on Silicon Carbide, III-Nitrides and Related Materials] (1997). n+ It is p+ by the ion implantation of high acceleration voltage [ surface layer / of n drift layer 21b by which the laminating was carried out on substrate 21a ]. The embedding field 22 is formed. The p+ It is n+ to the surface layer of n drift layer part 21b on the embedding field 22. The source field 23 is formed. Two n+ The gate electrode 26 is formed through gate dielectric film 25 on the front face of n drift layer part 21b inserted into the source field 23. n+ The source electrode 27 is n+ to the front face of the source field 23. The drain electrode 28 is formed in the rear face of substrate 21a, respectively.

[0006] In this example, the gate part has metal-oxide-semiconductor structure which impresses an electrical potential difference through gate dielectric film 25 instead of pn junction. In this MOSFET, by impressing a forward electrical potential difference to the gate electrode layer 26, induction of the accumulation layer is carried out to the n channel field 30 of the surface part of n drift layer 21b of gate electrode 26 directly under, and a current flows between the drain electrode 28 and the source electrode 27. Moreover, if a negative electrical potential difference is impressed to the gate electrode 26, the current between the drain electrode 28 and the source electrode 27 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 22 and n drift layer 21b, and to hold a big electrical potential difference, and it is made the structure suitable for high pressure-proofing. Since this MOSFET forms an accumulation layer by electrical-potential-difference impression to the gate electrode 26, it is called ACCUFET.

[0007] Drawing 15 is [ and Phys.Stat.Sol. (a) besides Onda and S., vol.162, and p.369] (1997) which are the fragmentary sectional view of the unit cell of another vertical mold quantity proof-pressure MOSFET \*\*. n+ The p base region 32 is formed on substrate 31a at the surface layer of n drift layer 31b by which the laminating was carried out, and it is n+ to the surface layer of the p base region 32. The source field 33 is formed. Two n+ The n channel field 40 which connects the source field 33 is formed of epitaxial growth, and the gate electrode layer 36 is formed through gate dielectric film 35 on the front face of the n channel field 40. n+ The source electrode 27 is n+ to the front face of the source field 33. The drain electrode 38 is formed in the rear face of substrate 31a, respectively.

[0008] By impressing a forward electrical potential difference to the gate electrode layer 36 also in this case, induction of the accumulation layer is carried out to the surface part of the n channel field 40 of gate electrode layer 36 directly under, and it becomes possible to pass the current from the drain electrode 38 to the source electrode 37. Moreover, between the drain electrode 38 and the source electrodes 27 will be intercepted, and by impressing a negative electrical potential difference to the gate electrode layer 36 will show a switching function.

[0009] Otherwise, although there is also an example of a prototype of MOSFET of a planar mold or a trench mold, by SiC, that the mobility of an inversion layer is very small gets down that it is experimentally sudden, and it is thought that FET of the enhancement type using an inversion layer is not suitable for practical use. It is the example of the structure where have the common description in that it is not FET of the enhancement type with which the component of the three above-mentioned examples uses an inversion layer to it but FET using the semi-conductor layer

of a conductivity type from the first as a channel, especially it is suitable for SiC.

[0010]

[Problem(s) to be Solved by the Invention] When it is going to manufacture the semiconductor device for power, the actual former not much good property is not realized, or the structure of drawing 13 , and 14 or drawing 15 is not manufactured in fact, although the property which was very excellent is expected. It is the double diffusion MOS (D-MOS) whose one of the reason of the is an approach which has spread most with Si semi-conductor. Structure is in an easily unrealizable point in SiC. In Si, a precise channel consistency is realized by introducing p mold impurity and n mold impurity alternatively with the same mask, and carrying out thermal diffusion. Namely, the dimension of the channel which influences the property of MOSFET is very controllable to a precision, and can make MOSFET with the sufficient yield.

[0011] It receives that can come and it is alike, and by SiC, the rate of activation of the impurity which carried out the ion implantation is bad, in order to raise this, an ion implantation 1000 degrees C or more and heat-of-activation processing at 1600 degrees C or more are required, and the diffusion of an impurity which carried out the ion implantation hardly breaks out. Therefore, installation of p mold impurity and n mold impurity must be depended on a respectively separate mask, and control of a precise channel consistency is not realized. Therefore, it becomes the thing also with the very big variation which has large channel resistance, and resistance of the whole component is like [ as which it will be mostly specified by channel resistance ]. It can be said that the property of SiC original is not acquired.

[0012] In view of the above problem, the purpose of this invention can realize a very precise channel, and is to offer the manufacture approach of silicon carbide vertical FET and silicon carbide vertical FET which can be high-pressure=proofed easily.

[0013]

[Means for Solving the Problem] The first conductivity-type drift layer which this invention becomes from the silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate for the above-mentioned technical-problem solution, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate some of one [ of the first mask ] edges -- one edge of the first conductivity-type source field -- specifying -- some other ends of the first mask, and other parts of the first mask -- the second conductivity-type gate field -- \*\* -- probably -- \*\* -- Other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0014] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first



conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0015] If it is made such, since the substantial dimension of a channel field is decided in the second conductivity-type gate field, the ununiformity by mask alignment will be avoided and precise control will be attained. It is possible for this to manufacture small FET of on resistance. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0016] Also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation is especially performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. The electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer may be prepared.

[0017] If it is made such, it can consider as a channel field smaller than the dimension of the second conductivity-type gate field required for contact resistance. Moreover, the first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate One edge of the first conductivity-type source field shall be specified with a part of first mask, and other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0018] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first

mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0019] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0020] A part with the thickness of the first mask of the shape of a taper with a loose edge thick as an option can prescribe one edge of the first conductivity-type source field, and a part with the thin thickness of the first mask of said first mask can also prescribe the edge of the second conductivity-type base region. For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the first mask of the shape of a taper with a loose edge, and the process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, It shall consist of the process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, the process which covers an insulator layer, a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0021] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. And another mask for impurity range formation is not needed. The crevice which arrives at the second conductivity-type base region from the front face of the first conductivity-type source field may be formed, and the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field may be prepared.

[0022] It is good to add the impurity installation process for the second conductivity-type contact field formation by using as a mask the process which prepares a sidewall in the side of the first mask especially, and the first mask and sidewall. If it is made such, it will not be based on mask alignment but formation of the second conductivity-type base region and the shifted second conductivity-type contact field can be performed.

[0023] The third mask with the thick thickness for the second conductivity-type contact field formation is formed, after passing through the process which introduces an impurity with the mask previously, etchback of the third mask can be carried out, and an edge can consider as the first mask of the shape of a loose taper. If it is made such, the first mask and third mask of a basis will be the same, and will not have the need of forming another mask ingredient.

[0024] Furthermore, also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation is performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. And the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer shall be added.

[0025] By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU. The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate by the above manufacture approaches, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, The source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, If it considers as the silicon carbide end-fire array FET which becomes shallow almost linearly so that it has the drain electrode prepared in the rear face of a silicon carbide substrate and the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field Control of the die length of a channel field is easy, and the end-fire array FET with a uniform channel field can manufacture easily.

[0026] From the second conductivity-type base region, even if it prepares the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region and contacts a source electrode on the front face of the second conductivity-type contact field with high high impurity concentration, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared, and a source electrode may be contacted on the exposure front face of the second conductivity-type contact field, so that a part may overlap the second conductivity-type base region.



[0027] If there is no need of preparing a crevice if a source electrode is contacted on the front face of the second conductivity-type contact field on the same front face as the first conductivity-type source field, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared and a source electrode is contacted, there will be no need of thickening thickness of the second conductivity-type contact field. By controlling the thing which is high concentration, then high impurity concentration from that of the first conductivity-type drift layer, the high impurity concentration of a channel field can control threshold voltage, and can set to FET of no MARIOFU.

[0028]

[Embodiment of the Invention] Below, this invention is explained to a detail, while an example is shown. However, explanation is omitted about drawing 13 -15, a common part, or a part without this invention or instead of. Although n channel MOS FET is taken for the example as an important application of this invention, of course, this invention can be adapted also for p channel MOS FET which made the conductivity type reverse. In addition, the silicon carbide explained here is aimed at what is mainly called 6H and 4H, although many polytypes exist as known well.

[0029] [Example 1] drawing 1 is the first example (it is described as an example 1 below.) of this invention. the following -- being the same -- it is the sectional view of the unit cell of starting SiCJFET. This supports the component which formed the conventional component of drawing 13 into high pressure-proofing. n+ It sets to the wafer with which the laminating of the n drift layer 41b was carried out by epitaxial growth on substrate 41a, and is p+ from the front face of n drift layer 41b to a somewhat deep location. The embedding field 42 is formed and it is p+. In the surface layer of upper n drift layer 41b of the embedding field 42, they are p gate field 44 and n+. The source field 43 is formed. The gate electrode 46 is formed on the front face of p gate field 44. n+ From the front face of the source field 43, the front face of investigated crevice 47a is met, and it is n+. The source field 43 and p+ It contacts common to a front face with the embedding field 42, and the source electrode 47 is formed, and it is n+. The rear face of substrate 41a is contacted and the drain electrode 48 is formed.

[0030] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of  $1 \times 10^{18} \text{cm}^{-3}$  in 350 micrometers in 3 and thickness and n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$  10 micrometers in 3 and thickness. p+ The highest high impurity concentration of the embedding field 42 is  $5 \times 10^{18} \text{cm}^{-3}$  0.5 micrometers in 3 and thickness, and n 0.5-micrometer drift layer 41b is on it. p+ of both sides Spacing between the embedding fields 42 is about 5 micrometers. n+ The high impurity concentration of the source field 43 is  $1 \times 10^{19} \text{cm}^{-3}$  3 and a junction depth of 0.2 micrometers, and width of face is [ 3 and a junction depth of 0.2 micrometers of  $5 \times 10^{18} \text{cm}^{-3}$ , and the width of face of it of about 3 micrometers and p gate field 44 ] about 2 micrometers. n+ Spacing between the source field 43 and p gate field 44 is about 1 micrometer, and n drift layer 41b has arrived at the front face. The depth of crevice 47a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 25 micrometers.

[0031] Although the point different from the horizontal type JFET of drawing 13 is a point that the source electrode 47 and the drain electrode 48 serve as FET of the vertical mold formed in both sides of a semi-conductor substrate, the actuation is not fundamentally different from the thing of drawing 11 . That is, a depletion layer is breadth and n+ by impressing an electrical potential difference to the gate electrode 46 to the channel field 50 of p gate field 44 to a lower part. The source field 43 and n drift layer 41b are insulated electrically. As a result, the current

from the drain electrode 38 to the source electrode 37 is controlled. It is JFET same depression type as what was shown in drawing 13.

[0032] Drawing 2 (a) thru/or (f) and drawing 3 (a) thru/or (d) are the fragmentary sectional views near the front face of the order of a production process for explaining the manufacture approach of SiCJFET of the example 1 of drawing 1. It explains in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 41b of a phosphorus dope with epitaxial growth is prepared on substrate 41a. For example, the high impurity concentration of n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$ , and thickness is 10 micrometers. On the front face of the n drift layer 41b, the polycrystal silicone film 1 is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [ drawing 2 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. Thickness of the polycrystal silicone film 1 was set to 1 micrometer. The first mask M1 does not necessarily need to be a polycrystal silicone film, and as long as it turns into a mask of alternative etching, it may be the oxidization silicon film (henceforth, SiO<sub>2</sub> it is described as the film) well used for a silicon process etc., the nitriding silicon film, or a photoresist. However, to carry out an ion implantation at an elevated temperature, it is necessary to use the ingredient which ceases to the elevated temperature of polycrystalline silicon etc.

[0033] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of the polycrystal silicone film 1. After depositing the film 2, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, nitrogen (it is described as Following N) ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [ these ] [this drawing (b)]. 4b is poured-in N atom. This is n+. It is for source field 43 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . The temperature at the time of an ion implantation is about 800 degrees C. The rate of activation can be raised by carrying out an ion implantation at an elevated temperature. The second mask M2 is not necessarily SiO<sub>2</sub>. Although it is not necessary to be the film, since it is required to remove leaving the first mask M1 at a next process, it considers as a different ingredient from the first mask M1, and it can be necessary to be made to perform alternative etching. For example, when a polycrystal silicone film is used as the first mask M1, it is SiO<sub>2</sub> like the upper example as the second mask M2. If the film is used, only the second mask 2 is removable with fluoric acid. It is SiO<sub>2</sub> by reactive ion etching (it is described as Following RIE) the reverse is also possible and using the mixed gas of a carbon tetrachloride and oxygen etc. in that case. It is possible to control the etch rate of the film and a polycrystal silicone film, and to etch only a polycrystal silicone film. Thus, alternative removal is just performed to the first mask M1. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, phosphorus (it is described as Following P) etc. is used other than N.

[0034] SiO<sub>2</sub> The second membranous mask M2 is removed and it is SiO<sub>2</sub> by the heat CVD method again. After depositing the film 2, forming a pattern by the photolithography and considering as the third mask M3, the ion used as p mold impurity, for example, boron (it is described as Following B) ion 5a, is poured into the field specified with the third mask M1 and M3 for a start [ these ] [this drawing (c)]. 5b is poured-in B atom. This is for p gate field 44 formation, acceleration voltage is 100keV(s) and a dose is abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . Also in this case, the third mask M3 is not necessarily SiO<sub>2</sub>. It is not necessary to be the film and alternative removal is just performed to the first mask M1 at a next process. Since the third mask M3 should just have an edge on the first mask M1, it is easy mask alignment. As p mold impurity and a becoming impurity, aluminum (it is described as Following aluminum) etc. can be used other

than B.

[0035] SiO<sub>2</sub> the third membranous mask M3 -- removing -- a photolithography -- \*\* -- a part of first mask -- M1b -- removing -- a part of first mask -- [this drawing (d)] which leaves M1a. a part of first mask which it left -- M1a is used as a mask and B ion 5a is poured in again. [This drawing (e)]. This is p+. It is for embedding field 42 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . Acceleration voltage was raised for forming a deep impurity range. As a p mold impurity, aluminum etc. may be used other than B.

[0036] a part of first mask which it left -- M1a is removed and N ion 4a is poured into the whole surface. [This drawing (f)]. 4b is poured-in N atom. This is for concentration control of the n channel field 50, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . Before this, it is p+. Since the deep ion implantation for the embedding field 42 is performed, it is p+. B atom is poured into n drift layer 41b of the surface layer which comes on the embedding field 42. Resistance of a surface layer can be stabilized by impregnation of N ion. The high impurity concentration of the surface layer after heat treatment is abbreviation  $5 \times 10^{15} \text{cm}^{-3}$ . It becomes.

[0037] It is n+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The source field 43, p gate field 44, and p+ Each field of the embedding field 42 is formed [ drawing 3 (a)]. Although diffusion of an impurity hardly breaks out in SiC as stated previously, the depth in which an impurity range is formed is controllable by accommodation of acceleration voltage. For example, p+ The embedding field 42 is made by the layer with a thickness of 0.5 micrometers at focusing on a depth of 0.8 micrometers by having made acceleration voltage high with 400keV(s), and n about 0.5-micrometer drift region 41b is left behind on it. p gate field 44 and n+ The depth of the source field 43 is about 0.2 micrometers.

[0038] To a front face, it is SiO<sub>2</sub> by the CVD method. The film 2 is deposited [this drawing (b)]. It is n+ at RIE form the fourth mask M4 by the photolithography, and using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>). Crevice 47a which arrives at p+ embedding field 42 from the front face of the source field 43 is formed [this drawing (c)]. It is SiO<sub>2</sub> at a photolithography. After forming opening for contact in the film 2 Pattern formation of the aluminium alloy film is vapor-deposited and carried out, and it considers as the source electrode 47 and the gate electrode 46., n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].

[0039] By taking the above manufacture approaches, it was able to consider as the high proof-pressure SiC vertical mold JFET of drawing 1 . SiCJFET of an example 1 -- a part of first mask - the edge of M1b -- n+ the source field 43 specifies -- having -- a part of first mask -- p gate field 44 is prescribed by another edge of M1b, and another partial M1a of the first mask. By partial M1a with the first still more nearly another mask, it is p+. The edge of the embedding field 42 is specified. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. After the pattern formation of the first mask M1, the advantage that the dimension of each impurity range can be checked is also.

[0040] Although the control is very important on application since the die length of a channel field is a main parameter which determines the property of MOSFET, in SiCJFET of this example 1, the n channel field 50 of the lower part of p gate field 44 serves as channel length substantially, channel length is formed with a precision short and sufficient to homogeneity, and the stable property and the high yield are obtained. The on resistance of JFET of 1500V class



made as an experiment showed 15m ohm-cm <sup>-2</sup> and a low value.

[0041] Moreover, p+ The embedding field 42 was formed by the ion implantation with high acceleration voltage, the junction depth was written deeply, and high pressure-proofing beyond 1500V has been realized easily. By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 41b, the threshold voltage of MOSFET can be controlled and it can also be referred to as FET of no MARIOFU.

[0042] Some deformation is also considered as the manufacture approach. For example, n+ Reverse is sufficient as the sequence of the ion implantation for forming the source field 43 and p gate field 44. Moreover, the ion implantation for high-impurity-concentration control of the n channel field 50 may be performed first. If it will carry out at low temperature more instead of an elevated temperature which calls an ion implantation 1000 degrees C, the selection width of face of a mask ingredient can extend.

[0043] [Example 2] drawing 4 is the fragmentary sectional view of SiCJFET concerning the second example of this invention. This is the modification of the example 1 of drawing 1 . A crevice is not formed in a SiC substrate front face in this example, but it is p+ to the surface layer of n drift layer 51b. p+ which arrives at the embedding field 52 Contact field 52a is formed and it is n+ to that front face. The source field 53 and the common source electrode 57 are formed.

[0044] n+ As a mask (it is equivalent to M2 of drawing 2 (b)) in the case of N ion implantation for source field 53 formation, it is n+. The mask which also specifies the outside of the source field 53 is used, still more nearly another mask is used, and it is p+. What is necessary is just to perform B ion implantation for contact field 52a formation. If it does in this way, a crevice cannot be formed but an electrode can be prepared in a substrate front face.

[0045] n+ There is instead of [ no ] in a part of first mask (it being equivalent to M1b of drawing 2 (b)) specifying the inside of the source field 53, and the die length of a channel field is the same as that of SiCJFET of an example 1, the n channel field 60 of the lower part of p gate field 44 has short uniform channel length, it is form with a sufficient precision, and the stable property and the high yield are obtain.

[0046] [Example 3] drawing 5 is the fragmentary sectional view of SiCJFET concerning the third example of this invention. This can also say it also as deformation of SiCJFET of drawing 1 . The point different from SiCJFET of drawing 1 is a point that the gate electrode 66 touches common to p gate field 64 and the front face of n drift layer 61b. Here, the gate electrode 66 chooses a SiC substrate and a metal which forms the Schottky barrier, for example, Ti, aluminum, Pt, etc.

[0047] At JFET of an example 1, as for p gate field 44, contact is taken only in the part which the gate electrode 46 contacts so that drawing 1 may show. In order to stop this contact resistance small, the touch area had to be enlarged and the magnitude of this contact aperture had restricted the minimum value of the die length of a channel. Since JFET of this example 3 improves this point and the gate electrode 66 touches not only p gate field 64 but the front face of n drift layer 61b, a large contact part can be taken and it becomes possible to design a channel field narrowly.

[0048] It also sets to JFET of this example 3, and is n+. It is the same that the property which a source field carries out self align to the surface layer of p base region, and is formed, and channel length was formed with a uniformly and sufficient precision like JFET of an example 1, and was stabilized is acquired with the sufficient yield. However, the gate electrodes 66 are a SiC substrate and the metal which forms the Schottky barrier, and are not necessarily the same metal as the source electrode 67. Or the gate electrode 66 may be made into a bilayer with the same metal as the metal and the source electrode 67 which carry out Schottky contact. About the

process which manufactures this, it is almost almost the same as that of drawing 2 and 3, and explanation is omitted.

[0049] [Example 4] drawing 6 is the fragmentary sectional view of SiCMOSFET concerning the fourth example of this invention. n+ In the wafer with which the laminating of the n drift layer 71b was carried out by epitaxial growth on substrate 71a It is p+ from the front face of n drift layer 71b to a somewhat deep location. The embedding field 72 is formed and it is the p+. It is n+ to the surface layer of upper n drift layer 71b of the embedding field 72. Although the point that the source field 73 is formed is the same as an old example There is nothing and p gate field is p+. The upper part of the embedding field 72 is made into the n channel field 80, and the gate of metal-oxide-semiconductor structure is prepared on the front face.

[0050] That is, the gate electrode layer 76 which consists of a polycrystalline silicon layer through gate oxide 75 is formed on the front face of n drift layer 71b. 79 is an insulator layer of boron phosphorus silica glass (BPSG) which insulates the gate electrode layer 76 and the source electrode 77. n+ There is crevice 77a investigated from the front face of the source field 73, the front face is met, and it is n+. The source field 73 and p+ The source electrode 77 which contacts common to a front face with the embedding field 72 is formed, and it is n+. The rear face of substrate 71a is contacted and the drain electrode 78 is formed. The dimension of main each part is almost the same as the value stated in the example 1. The thickness of gate oxide 75 is [ the thickness of 1 micrometer and an insulator layer 79 of the thickness of 50nm and the gate electrode layer 76 ] 2 micrometers.

[0051] When this MOSFET is also called ACCUFET and impresses a forward electrical potential difference to the gate electrode layer 76, induction of the accumulation layer is carried out to the surface part of n drift layer 71b of gate electrode layer 76 directly under, and a current flows between the drain electrode 78 and the source electrode 77. Moreover, if a negative electrical potential difference is impressed to the gate electrode layer 76, the current between the drain electrode 78 and the source electrode 77 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 72 and n drift layer 71b, and to hold a big electrical potential difference, and it has structure suitable for high pressure-proofing.

[0052] Drawing 7 (a) thru/or (e) and drawing 8 (a) thru/or (d) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 4 of drawing 6 . A process is explained in order of below. n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 71b of a phosphorus dope with epitaxial growth is prepared on substrate 71a. The high impurity concentration of n drift layer 71b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 71b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [ drawing 7 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0053] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of a polycrystal silicone film. After depositing the film, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, N ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [ these ] [this drawing (b)]. This is n+. It is for source field 73 formation, and acceleration voltage, a dose, etc. are the same as an example 1, and good. this second mask M2 -- not necessarily -- SiO<sub>2</sub> it is not necessary to be -- although -- since it is required to remove leaving the first mask M1 at a next process, unlike the first mask

M1, the ingredient which can perform alternative etching is chosen. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, P etc. is used other than N.

[0054] SiO<sub>2</sub> the second membranous mask M2 -- removing -- a photolithography -- a part of first mask -- [this drawing (c)] which pours in the ion used as p mold impurity, for example, B ion 5a, after leaving M1a. This is p<sup>+</sup>. It is for embedding field 72 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . Acceleration voltage was raised for forming a deep impurity range. As for p mold impurity, aluminum etc. is used other than B.

[0055] a part of first mask which it left -- M1a is removed and N ion 4a is poured in. [This drawing (d)]. This is for high-impurity-concentration control of the n channel field 80, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . It is p<sup>+</sup> by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The embedding field 72 and n<sup>+</sup> Each field of the source field 73 and the n channel field 80 is formed [this drawing (e)].

[0056] SiO<sub>2</sub> film which turns into gate oxide 75 by 1200 degrees C and thermal oxidation of 2 hours is formed in a front face, and about 1 micrometer of polycrystal silicone films 1 which serve as a gate electrode layer with a reduced pressure CVD method continuously is deposited [drawing 8 (a)]. It forms by thermal oxidation, and also gate oxide 75 can also form membranes by CVD. As an ingredient of the gate electrode layer 76, molybdenum (Mo) etc. is [ other than polycrystalline silicon ] usable.

[0057] A photoresist is applied, and after carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 76, the insulator layers 79, such as boron phosphorus silica glass (BPSG), are deposited on a front face with a CVD method [this drawing (b)]. It is n<sup>+</sup> at RIE form a pattern by the photolithography and using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>). The front face of the source field 73 to p<sup>+</sup> Crevice 77a which arrives at the embedding field 72 is formed [this drawing (c)].

[0058] After forming opening for contact in an insulator layer 79 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 77 and the gate electrode which is not illustrated. n<sup>+</sup> A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].

MOSFET of this example 4 -- also setting -- a part of first mask -- the edge of M1b -- n<sup>+</sup> The source field 73 is specified and the edge of p<sup>+</sup> embedding field 72 is prescribed by partial M1a with the first another mask. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise.

[0059] Therefore, like JFET of an example 1, about 1.5-micrometer channel length is realized with a uniformly and sufficient precision, and the stable property is acquired with the sufficient yield. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also. By being added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 71b, and considering as the n channel field 80, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU.

[0060] Moreover, since gate oxide 75 is formed on the SiC substrate at the plane, there is no problem of the stress of the electric field in the corner section of the gate oxide seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Some deformation is also



considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 80 may be performed first, and reverse order is sufficient as formation with the second mask M2 and the third mask M3.

[0061] n+ In the case of N ion implantation for source field 73 formation, it is n+. The mask which specifies the outside of the source field 73 is used, still more nearly another mask is used, and it is p+. If B ion implantation for contact field 52a formation is performed, crevice 77a cannot be formed but an electrode can be prepared in a substrate front face. In that case The die length of a channel field is formed in homogeneity with a sufficient precision like SiCMOSFET of an example 4, and the stable property and the high yield are obtained.

[0062] [Example 5] drawing 9 is the fragmentary sectional view of SiCMOSFET concerning the fifth example of this invention. n+ It is p+ to a somewhat deep location from the front face of n drift layer 81b deposited with epitaxial growth on substrate 81a. The embedding field 82 is formed and it is p+. The p base region 82 is formed in the surface layer of upper n drift layer 81b of the embedding field 82, and it is n+ alternatively in the upper part. The source field 83 is formed. And the part of the edge of the p base region 82 is n+. It is so characteristic that it keeps away from the source field 83 that the junction depth is shallow almost linearly. Moreover, it is p+ to a part deeper than the p base region 82 so that the p base region 82 may be overlapped in part. Contact field 82a is formed. n+ The upper part of the p base region 82 of a part in which the source field 83 is not formed is made into the n channel field 90, and the gate of the same metal-oxide-semiconductor structure as MOSFET of drawing 6 is prepared on it. That is, the gate electrode layer 86 which consists of a polycrystalline silicon layer through gate oxide 85 is formed. 89 is the insulator layer of BPSG which insulates a gate electrode layer and the source electrode 87. n+ From the front face of the source field 83, there is investigated crevice 87a and it is n+. The source field 83 and p+ It contacts common to a front face with the contact field 82, and the source electrode 87 is formed, and it is n+. The rear face of substrate 81a is contacted and the drain electrode 88 is formed.

[0063] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of  $1 \times 10^{18} \text{cm}^{-3}$  in 350 micrometers in 3 and thickness and n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$  10 micrometers in 3 and thickness. Spacing between 3 and a junction depth of 1.5 micrometers of  $5 \times 10^{16} \text{cm}^{-3}$ , and the p base region 82 of both sides of the highest high impurity concentration of the p base region 82 is about 6 micrometers. n+ The high impurity concentration of the source field 43 is  $1 \times 10^{19} \text{cm}^{-3}$  3 and a junction depth of 0.2 micrometers, and width of face is about 5 micrometers and p+. The highest high impurity concentration of the contact field 82 is [ the high impurity concentration of about 5 micrometers and the n channel field 90 of 3 and a junction depth of 2.0 micrometers of  $1 \times 10^{19} \text{cm}^{-3}$ , and width of face ]  $5 \times 10^{15} \text{cm}^{-3}$  3 and a junction depth of 0.5 micrometers. n+ Spacing between the edge of the source field 83 and the edge of the p base region 82 is about 2 micrometers. The depth of crevice 87a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 30 micrometers. The thickness of gate oxide 85 is [ the thickness of 1 micrometer and an insulator layer 89 of the thickness of 50nm and the gate electrode layer 86 ] 2 micrometers.

[0064] Drawing 10 (a) thru/or (e) and drawing 11 (a) thru/or (e) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 5 of drawing 9. A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 81b of a phosphorus dope with epitaxial growth is prepared on a substrate. On the front face of n drift layer 81b, a polycrystal silicone film is

deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1.

[0065] It is important especially in the case of this patterning to form the taper section 8 in the edge of the first mask M1 over 1-2 micrometers. This is because channel length is controlled by the include angle of the taper section 8 of the first mask M1 in the ion implantation for the next p base region formation. Therefore, this cone angle must be captured and decided to be a predetermined design. And this include angle is controllable by choosing the etching conditions at the time of etching the thin film of the first mask 1 by plasma etching etc. Or a loose taper will be obtained, if an ion implantation is carried out to the upper part of a thin film, the damage is given to it and it carries out only near the front face that it is easy to be etched. There is also the approach of controlling a taper angle by controlling the dose of the ion implantation in that case.

[0066] The ion, for example, boron (B) ion 5a, which serves as p mold impurity by using the first mask M1 as a mask is poured in [ drawing 10 (a)]. 5b is poured-in B atom. This is for p base region 82 formation, acceleration voltage is 300keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . Acceleration voltage was raised for forming a deep impurity range. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow almost linear gradually as thickness of the mask [ first ] M1 increases, and an impurity atom carries out distribution as shown in drawing. If thickness of the first mask M1 is made to some extent thin, an impurity impregnation field does not arrive at even a front face, but can be made into the field of an embedding mold. As for p mold impurity, aluminum etc. is used other than B. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0067] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using the first same mask M1 as a mask is poured in [this drawing (b)]. 4b is poured-in n atom. This is for n+ source field 83 formation, and the 100keV(s) as an example 1 with the same acceleration voltage etc. and a dose are good at abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . In the field which does not have the first mask M1 in this case, either, an impurity is poured in deeply, if the first mask M1 becomes thick, it will become shallow gradually, and an impurity atom carries out distribution as shown in drawing. However, since acceleration voltage is made low, the field poured in differs from the impregnation field of B ion. If the include angle of the taper section 8 is the same, spacing of the impregnation field of p mold impurity and the impregnation field of n mold impurity will become fixed.

[0068] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of a polycrystal silicone film. The film 2 is deposited [this drawing (c)]. After forming a sidewall 9 in the side of \*\* and the taper section 8 of the first mask M1 carrying out overall etching by RIE, the ion used as p mold impurity, for example, B ion 5a, is poured into the field specified by these first masks M1 and the sidewall 9 [this drawing (d)]. This is high-concentration p+. It is for contact field 84 formation, and acceleration voltage, 400keV, and a dose are abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . As a p mold impurity, aluminum etc. is used other than B.

[0069] After removing the first mask M1 and a sidewall 9, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field 90, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . Thereby, a threshold is controllable. Each field is formed by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity [ drawing 11 (a)]. Thus, p base region 82sn+ The source field 83 can be shifted and formed.

[0070] Heat SiO<sub>2</sub> with a thickness of 50nm it is thin to gate oxide 85 on a front face with 1200

degrees C and thermal oxidation of 2 hours The film 6 is formed, and about 1 micrometer of polycrystal silicon films 1 is continuously deposited with a reduced pressure CVD method [this drawing (b)]. It forms by thermal oxidation, and also gate oxide 85 can also form membranes by CVD. After applying a photoresist, carrying out pattern formation of the polycrystal silicon film 1 by the photolithography and considering as the gate electrode layer 86, with a CVD method, the insulator layers 89, such as boron phosphorus silica glass (BPSG), are deposited on a front face, and a pattern is formed in it by the photolithography [this drawing (c)].

[0071] At RIE using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>), it is p+ from the front face of n+ source field 83. Crevice 87a which reaches contact field 82a is formed [this drawing (d)]. After forming opening for contact in an insulator layer 89 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 87 and the gate electrode which is not illustrated [this drawing (e)]. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed.

[0072] In MOSFET of this example 5, the edge of n+ source field 83 and the p base region 82 is prescribed by by making the edge of the first mask 1 into the shape of a taper, and changing the acceleration voltage in the case of impregnation of p mold impurity and n mold impurity. That is, the channel length who is spacing between both is prescribed by the taper section 8 of the first mask M1. Thus, since the impurity range is prescribed by only the first mask, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, does not occur.

[0073] Therefore, channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield. Moreover, if the include angle of the taper section 8 of the first mask M1 is changed, both spacing, i.e., the die length of a channel field, can be controlled freely, and the balance of on resistance and pressure-proofing will also tend to take it. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also.

[0074] By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 81b, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 90 may be performed first. Moreover, impregnation and n+ of B ion for the p base region 82 Reverse is sufficient as the order of impregnation of N ion for source field 83 formation. A sidewall field is formed first and it is p+. The ion implantation for contact field 84 formation may be performed.

[0075] Since gate oxide 85 is formed on the SiC substrate also in this example at the plane, there is no problem of the stress of the electric field in the gate oxide corner section seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Moreover, at this example, it is p+. It is n+, although contact field 82a was embedded and being considered as the field of a mold. In the case of N ion implantation for source field 83 formation, it is n+. The mask which specifies the outside of the source field 83 is used, and it is p+. If contact field 82a is made to arrive at even a front face by multiplex impregnation, the source electrode 87 can be formed in a substrate front face, and there will be no need of forming crevice 87a.

[0076] [Example 6] drawing 12 (a) thru/or (e) are the fragmentary sectional views near the front face of the order of a production process for explaining the another manufacture approach of the almost same SiCMOSFET as SiCMOSFET of drawing 9 . A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 91b of a



phosphorus dope with epitaxial growth is prepared on a substrate. The high impurity concentration of n drift layer 91b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 91b, it is SiO<sub>2</sub> with a thickness of about 2 micrometers by the plasma-CVD method. The film 2 is deposited, a pattern is formed by the photolithography, and it considers as the third mask M3.

[0077] The ion, for example, B ion 5a, which serves as p mold impurity by using the third mask M3 as a mask is poured in [ drawing 12 (a)]. 5b is poured-in B atom. This is high-concentration p+. It is for contact field 94 formation, and acceleration voltage, 400keV, and a dose are abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . As a p mold impurity, aluminum etc. is used other than B.

[0078] Next, CF<sub>4</sub>+H<sub>2</sub> It considers as the first mask M1 which carried out etchback of the third mask M3, and made the edge the shape of a taper over 1-2 micrometers by plasma etching using gas [this drawing (b)]. At this time, the whole thickness also becomes thin and thickness is set to about 1 micrometer. In the ion implantation for the next p base region formation, a channel is controlled by the cone angle of the edge of the first mask by this like the time of SiCMOSFET of an example 5.

[0079] The ion, for example, B ion 5a, which serves as p mold impurity by using as a mask the first mask M1 which made the edge the shape of a taper is poured in [this drawing (c)]. This is for p base region 92 formation, acceleration voltage is 300keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow gradually as thickness of the mask [ first ] M1 increases, and an impurity atom carries out distribution as shown in drawing.

[0080] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using as a mask the first mask M1 which made the same edge the shape of a taper is poured in [this drawing (d)]. This is n+. It is for source field 93 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . Since acceleration voltage is made low, the field poured in differs from the impregnation field of p mold impurity.

[0081] After removing the first mask M1, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field of the surface layer of n drift layer 91b, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . Thereby, a threshold is controllable. After this, activation of the impurity poured in after drawing 10 (a), formation of an electrode, etc. are performed.

[0082] Since back dirty [ of the third mask M3 ] was carried out and it considered as the first mask M1 when taking this approach, it is not necessary to form a mask ingredient anew. And since the include angle of the taper section also becomes homogeneity and spacing of the p base region 92 and n source field 93 is specified, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. And channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield.

[0083] Some deformation is also considered as the manufacture approach. For example, a reverse order is sufficient as impregnation [ drawing 12 (c)] of p mold impurity ion for p base region formation, and impregnation [ drawing 12 (d)] of n mold impurity ion for n source field formation, and the ion implantation for high-impurity-concentration control of an n channel field [ drawing 12 (e)] may be performed first.

[0084]

[Effect of the Invention] As explained above, according to this invention, it sets to the manufacture approach of silicon carbide vertical FET. Some of one [ of the first mask ] edges

prescribe the first conductivity-type impurity installation field using the first mask and the second mask which overlaps in part. By removing the first some masks and second mask, and specifying the second conductivity-type impurity installation field by another part of the first mask, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field are formed in self align.

[0085] If the approach of changing and carrying out the ion implantation of the acceleration voltage is taken using the mask which made especially the edge the shape of a taper, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field can be formed in self align only with one mask. By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU.

[0086] Thus, JFET and MOSFET with the former very difficult very precise channel field can be realized now, and effectiveness was brought to reduction of on resistance. This invention is an approach very effective not only in FET according to individual but CMOS-IC and other SiC semiconductor devices, and makes easy manufacture of the silicon carbide semiconductor device of high pressure-proofing.

---

[Translation done.]

**\* NOTICES \***

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

**TECHNICAL FIELD**

---

[Field of the Invention] This invention relates to the manufacture approach of a vertical mold field-effect transistor (it is described as Following FET) and the vertical mold electric field effect FET with the gate of the assembling die which used silicon carbide as a semiconductor material and which is a power semiconductor device, or the MOS mold of metal-oxide film-semiconductor structure.

---

[Translation done.]



**\* NOTICES \***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

**PRIOR ART**

[Description of the Prior Art] Since a band gap is large and the maximum insulation electric field are large a figure single [ about ] as compared with silicon (it is described as Following Si), silicon carbide (it is described as Following SiC) is an ingredient with which the application to a next-generation power semiconductor device is expected. It is applied to various electron devices until now using the single crystal wafer called 4 H-SiC or 6 H-SiC, and it is thought that it is especially suitable for an elevated temperature and the component for large power. The above-mentioned crystal is the alpha phase SiC of the form which carried out the laminating of a sphalerite mold and the wurtzite mold. The semiconductor device is made also for the crystal of the beta phase SiC otherwise called 3 C-SiC as an experiment. [ , for example, Weitzel, by which CMOS-IC which is the general-purpose semiconductor devices, such as schottky diode, end-fire array MOSFET, and a thyristor, as a component for power is recently made as an experiment, and it is checked from the property as compared with the conventional Si semiconductor device that a property is very good, :IEEE Trans.on Electron Devices besides C.W., and vol. -- 43, No.10, and pp.1732-1741 --] (1997) . Some examples of MOSFET are shown below.

[0003] Drawing 13 is the fragmentary sectional view of the unit cell of junction type FET (it omits Following JFET) currently developed as one of the RF components [ and Abstracta of Int.Conf.on Silicon Carbide besides Sheppard and S.T., III-Nitrides and Related Materials] (1997). p+ It is n+ to the surface layer of n drift layer 11 by which the laminating was carried out on the substrate 10. The source field 13, p gate field 15, and n+ The drain field is formed. n+ The source field 13 and n+ The drain field 14 and p gate field 15 are contacted, and the source electrode 17, the drain electrode 18, and the gate electrode 16 are formed, respectively.

[0004] When an electrical potential difference is impressed to the gate electrode 16 with this structure, they are p gate field 15 to p gate field 15, and p+. A depletion layer spreads to the n channel field 20 between substrates 10. The current between the source electrode 17 and the drain electrode 18 is controlled by this. Moreover, a current flows again between the drain electrode 18 and the source electrode 17 by removing the electrical potential difference impressed to the gate electrode 16. Thus, the current between source drains serves as a component switchable [ with gate voltage ]. Since this JFET depletion-izes a channel field by electrical-potential-difference impression to the gate electrode 16, it is called a depletion type. A front face to p+ The slot which reaches a substrate 10 is formed and it fills up with the insulator layer 19 because [ of isolation ].

[0005] On the other hand, drawing 14 is one sort of a vertical mold MOSFET [Shenoy, J.N. others , Abstracta of Int.Conf.on Silicon Carbide, III-Nitrides and Related Materials] (1997). n+ It is p+ by the ion implantation of high acceleration voltage [ surface layer / of n drift layer 21b by which the laminating was carried out on substrate 21a ]. The embedding field 22 is formed. The p+ It is n+ to the surface layer of n drift layer part 21b on the embedding field 22. The

source field 23 is formed. Two n+ The gate electrode 26 is formed through gate dielectric film 25 on the front face of n drift layer part 21b inserted into the source field 23. n+ The source electrode 27 is n+ to the front face of the source field 23. The drain electrode 28 is formed in the rear face of substrate 21a, respectively.

[0006] In this example, the gate part has metal-oxide-semiconductor structure which impresses an electrical potential difference through gate dielectric film 25 instead of pn junction. In this MOSFET, by impressing a forward electrical potential difference to the gate electrode layer 26, induction of the accumulation layer is carried out to the n channel field 30 of the surface part of n drift layer 21b of gate electrode 26 directly under, and a current flows between the drain electrode 28 and the source electrode 27. Moreover, if a negative electrical potential difference is impressed to the gate electrode 26, the current between the drain electrode 28 and the source electrode 27 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 22 and n drift layer 21b, and to hold a big electrical potential difference, and it is made the structure suitable for high pressure-proofing. Since this MOSFET forms an accumulation layer by electrical-potential-difference impression to the gate electrode 26, it is called ACCUFET.

[0007] Drawing 15 is [ and Phys.Stat.Sol. (a) besides Onda and S., vol.162, and p.369] (1997) which are the fragmentary sectional view of the unit cell of another vertical mold quantity proof-pressure MOSFET \*\*. . n+ The p base region 32 is formed on substrate 31a at the surface layer of n drift layer 31b by which the laminating was carried out, and it is n+ to the surface layer of the p base region 32. The source field 33 is formed. Two n+ The n channel field 40 which connects the source field 33 is formed of epitaxial growth, and the gate electrode layer 36 is formed through gate dielectric film 35 on the front face of the n channel field 40. n+ The source electrode 27 is n+ to the front face of the source field 33. The drain electrode 38 is formed in the rear face of substrate 31a, respectively.

[0008] By impressing a forward electrical potential difference to the gate electrode layer 36 also in this case, induction of the accumulation layer is carried out to the surface part of the n channel field 40 of gate electrode layer 36 directly under, and it becomes possible to pass the current from the drain electrode 38 to the source electrode 37. Moreover, between the drain electrode 38 and the source electrodes 27 will be intercepted, and by impressing a negative electrical potential difference to the gate electrode layer 36 will show a switching function.

[0009] Otherwise, although there is also an example of a prototype of MOSFET of a planar mold or a trench mold, by SiC, that the mobility of an inversion layer is very small gets down that it is experimentally sudden, and it is thought that FET of the enhancement type using an inversion layer is not suitable for practical use. It is the example of the structure where have the common description in that it is not FET of the enhancement type with which the component of the three above-mentioned examples uses an inversion layer to it but FET using the semi-conductor layer of a conductivity type from the first as a channel, especially it is suitable for SiC.

---

[Translation done.]

**\* NOTICES \***

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. \*\*\*\* shows the word which can not be translated.

3. In the drawings, any words are not translated.

---

**EFFECT OF THE INVENTION**

---

[Effect of the Invention] As explained above, according to this invention, it sets to the manufacture approach of silicon carbide vertical FET. Some of one [ of the first mask ] edges prescribe the first conductivity-type impurity installation field using the first mask and the second mask which overlaps in part. By removing the first some masks and second mask, and specifying the second conductivity-type impurity installation field by another part of the first mask, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field are formed in self align.

[0085] If the approach of changing and carrying out the ion implantation of the acceleration voltage is taken using the mask which made especially the edge the shape of a taper, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field can be formed in self align only with one mask. By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU.

[0086] Thus, JFET and MOSFET with the former very difficult very precise channel field can be realized now, and effectiveness was brought to reduction of on resistance. This invention is an approach very effective not only in FET according to individual but CMOS-IC and other SiC semiconductor devices, and makes easy manufacture of the silicon carbide semiconductor device of high pressure-proofing.

---

[Translation done.]



**\* NOTICES \***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. \*\*\*\* shows the word which can not be translated.

3. In the drawings, any words are not translated.

---

**TECHNICAL PROBLEM**

---

[Problem(s) to be Solved by the Invention] When it is going to manufacture the semiconductor device for power, the actual former not much good property is not realized, or the structure of drawing 13, and 14 or drawing 15 is not manufactured in fact, although the property which was very excellent is expected. It is the double diffusion MOS (D-MOS) whose one of the reason of the is an approach which has spread most with Si semi-conductor. Structure is in an easily unrealizable point in SiC. In Si, a precise channel consistency is realized by introducing p mold impurity and n mold impurity alternatively with the same mask, and carrying out thermal diffusion. Namely, the dimension of the channel which influences the property of MOSFET is very controllable to a precision, and can make MOSFET with the sufficient yield.

[0011] It receives that can come and it is alike, and by SiC, the rate of activation of the impurity which carried out the ion implantation is bad, in order to raise this, an ion implantation 1000 degrees C or more and heat-of-activation processing at 1600 degrees C or more are required, and the diffusion of an impurity which carried out the ion implantation hardly breaks out. Therefore, installation of p mold impurity and n mold impurity must be depended on a respectively separate mask, and control of a precise channel consistency is not realized. Therefore, it becomes the thing also with the very big variation which has large channel resistance, and resistance of the whole component is like [ as which it will be mostly specified by channel resistance ]. It can be said that the property of SiC original is not acquired.

[0012] In view of the above problem, the purpose of this invention can realize a very precise channel, and is to offer the manufacture approach of silicon carbide vertical FET and silicon carbide vertical FET which can be high-pressure=proofed easily.

---

[Translation done.]

**\* NOTICES \***

**JPO and NCIP are not responsible for any damages caused by the use of this translation.**

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. \*\*\*\* shows the word which can not be translated.

3. In the drawings, any words are not translated.

---

**MEANS**

---

[Means for Solving the Problem] The first conductivity-type drift layer which this invention becomes from the silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate for the above-mentioned technical-problem solution, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate some of one [ of the first mask ] edges -- one edge of the first conductivity-type source field -- specifying -- some other ends of the first mask, and other parts of the first mask -- the second conductivity-type gate field -- \*\* -- probably -- \*\* -- Other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0014] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which

forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0015] If it is made such, since the substantial dimension of a channel field is decided in the second conductivity-type gate field, the ununiformity by mask alignment will be avoided and precise control will be attained. It is possible for this to manufacture small FET of on resistance. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0016] Also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation is especially performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. The electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer may be prepared.

[0017] If it is made such, it can consider as a channel field smaller than the dimension of the second conductivity-type gate field required for contact resistance. Moreover, the first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate One edge of the first conductivity-type source field shall be specified with a part of first mask, and other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0018] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of a process



which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0019] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0020] A part with the thickness of the first mask of the shape of a taper with a loose edge thick as an option can prescribe one edge of the first conductivity-type source field, and a part with the thin thickness of the first mask of said first mask can also prescribe the edge of the second conductivity-type base region. For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the first mask of the shape of a taper with a loose edge, and the process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, It shall consist of the process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, the process which covers an insulator layer, a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0021] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. And another mask for impurity range formation is not needed. The crevice which arrives at the second conductivity-type base region from the front face of the first conductivity-type source field may be formed, and the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field may be prepared.

[0022] It is good to add the impurity installation process for the second conductivity-type contact field formation by using as a mask the process which prepares a sidewall in the side of the first mask especially, and the first mask and sidewall. If it is made such, it will not be based on mask alignment but formation of the second conductivity-type base region and the shifted second conductivity-type contact field can be performed.

[0023] The third mask with the thick thickness for the second conductivity-type contact field formation is formed, after passing through the process which introduces an impurity with the mask previously, etchback of the third mask can be carried out, and an edge can consider as the

first mask of the shape of a loose taper. If it is made such, the first mask and third mask of a basis will be the same, and will not have the need of forming another mask ingredient.

[0024] Furthermore, also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation is performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. And the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer shall be added.

[0025] By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU. The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate by the above manufacture approaches, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, The source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, If it considers as the silicon carbide end-fire array FET which becomes shallow almost linearly so that it has the drain electrode prepared in the rear face of a silicon carbide substrate and the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field Control of the die length of a channel field is easy, and the end-fire array FET with a uniform channel field can manufacture easily.

[0026] From the second conductivity-type base region, even if it prepares the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region and contacts a source electrode on the front face of the second conductivity-type contact field with high high impurity concentration, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared, and a source electrode may be contacted on the exposure front face of the second conductivity-type contact field, so that a part may overlap the second conductivity-type base region.

[0027] If there is no need of preparing a crevice if a source electrode is contacted on the front face of the second conductivity-type contact field on the same front face as the first conductivity-type source field, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared and a source electrode is contacted, there will be no need of thickening thickness of the second conductivity-type contact field. By controlling the thing which is high concentration, then high impurity concentration from that of the first conductivity-type drift layer, the high impurity concentration of a channel field can control threshold voltage, and can set to FET of no MARIOFU.

[0028]

[Embodiment of the Invention] Below, this invention is explained to a detail, while an example is shown. However, explanation is omitted about drawing 13 -15, a common part, or a part without this invention or instead of. Although n channel MOS FET is taken for the example as an important application of this invention, of course, this invention can be adapted also for p channel MOS FET which made the conductivity type reverse. In addition, the silicon carbide

explained here is aimed at what is mainly called 6H and 4H, although many polytypes exist as known well.

[0029] [Example 1] drawing 1 is the first example (it is described as an example 1 below.) of this invention. the following -- being the same -- it is the sectional view of the unit cell of starting SiCJFET. This supports the component which formed the conventional component of drawing 13 into high pressure-proofing. n+ It sets to the wafer with which the laminating of the n drift layer 41b was carried out by epitaxial growth on substrate 41a, and is p+ from the front face of n drift layer 41b to a somewhat deep location. The embedding field 42 is formed and it is p+. In the surface layer of upper n drift layer 41b of the embedding field 42, they are p gate field 44 and n+. The source field 43 is formed. The gate electrode 46 is formed on the front face of p gate field 44. n+ From the front face of the source field 43, the front face of investigated crevice 47a is met, and it is n+. The source field 43 and p+ It contacts common to a front face with the embedding field 42, and the source electrode 47 is formed, and it is n+. The rear face of substrate 41a is contacted and the drain electrode 48 is formed.

[0030] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of  $1 \times 10^{18} \text{cm}^{-3}$  in 350 micrometers in  $\phi$  and thickness and n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$  10 micrometers in  $\phi$  and thickness. p+ The highest high impurity concentration of the embedding field 42 is  $5 \times 10^{18} \text{cm}^{-3}$  0.5 micrometers in  $\phi$  and thickness, and n 0.5-micrometer drift layer 41b is on it. p+ of both sides Spacing between the embedding fields 42 is about 5 micrometers. n+ The high impurity concentration of the source field 43 is  $1 \times 10^{19} \text{cm}^{-3}$  and a junction depth of 0.2 micrometers, and width of face is [  $\phi$  3 and a junction depth of 0.2 micrometers of  $5 \times 10^{18} \text{cm}^{-3}$ , and the width of face of it of about 3 micrometers and p gate field 44 ] about 2 micrometers. n+ Spacing between the source field 43 and p gate field 44 is about 1 micrometer, and n drift layer 41b has arrived at the front face. The depth of crevice 47a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 25 micrometers.

[0031] Although the point different from the horizontal type JFET of drawing 13 is a point that the source electrode 47 and the drain electrode 48 serve as FET of the vertical mold formed in both sides of a semi-conductor substrate, the actuation is not fundamentally different from the thing of drawing 11. That is, a depletion layer is breadth and n+ by impressing an electrical potential difference to the gate electrode 46 to the channel field 50 of p gate field 44 to a lower part. The source field 43 and n drift layer 41b are insulated electrically. As a result, the current from the drain electrode 38 to the source electrode 37 is controlled. It is JFET same depression type as what was shown in drawing 13.

[0032] Drawing 2 (a) thru/or (f) and drawing 3 (a) thru/or (d) are the fragmentary sectional views near the front face of the order of a production process for explaining the manufacture approach of SiCJFET of the example 1 of drawing 1. It explains in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 41b of a phosphorus dope with epitaxial growth is prepared on substrate 41a. For example, the high impurity concentration of n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$ , and thickness is 10 micrometers. On the front face of the n drift layer 41b, the polycrystal silicone film 1 is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [ drawing 2 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. Thickness of the polycrystal silicone film 1 was set to 1 micrometer. The first mask M1 does not necessarily need to be a polycrystal silicone film, and as long as it turns into a mask of alternative etching, it may be the oxidization silicon film (henceforth, SiO<sub>2</sub> it is described as the



film) well used for a silicon process etc., the nitriding silicon film, or a photoresist. However, to carry out an ion implantation at an elevated temperature, it is necessary to use the ingredient which ceases to the elevated temperature of polycrystalline silicon etc.

[0033] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of the polycrystal silicon film 1. After depositing the film 2, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, nitrogen (it is described as Following N) ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [ these ] [this drawing (b)]. 4b is poured-in N atom. This is n<sup>+</sup>. It is for source field 43 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation 5x10<sup>15</sup>cm<sup>-2</sup>. The temperature at the time of an ion implantation is about 800 degrees C. The rate of activation can be raised by carrying out an ion implantation at an elevated temperature. The second mask M2 is not necessarily SiO<sub>2</sub>. Although it is not necessary to be the film, since it is required to remove leaving the first mask M1 at a next process, it considers as a different ingredient from the first mask M1, and it can be necessary to be made to perform alternative etching. For example, when a polycrystal silicon film is used as the first mask M1, it is SiO<sub>2</sub> like the upper example as the second mask M2. If the film is used, only the second mask 2 is removable with fluoric acid. It is SiO<sub>2</sub> by reactive ion etching (it is described as Following RIE) the reverse is also possible and using the mixed gas of a carbon tetrachloride and oxygen etc. in that case. It is possible to control the etch rate of the film and a polycrystal silicon film, and to etch only a polycrystal silicon film. Thus, alternative removal is just performed to the first mask M1. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, phosphorus (it is described as Following P) etc. is used other than N.

[0034] SiO<sub>2</sub> The second membranous mask M2 is removed and it is SiO<sub>2</sub> by the heat CVD method again. After depositing the film 2, forming a pattern by the photolithography and considering as the third mask M3, the ion used as p mold impurity, for example, boron (it is described as Following B) ion 5a, is poured into the field specified with the third mask M1 and M3 for a start [ these ] [this drawing (c)]. 5b is poured-in B atom. This is for p gate field 44 formation, acceleration voltage is 100keV(s) and a dose is abbreviation 5x10<sup>15</sup>cm<sup>-2</sup>. Also in this case, the third mask M3 is not necessarily SiO<sub>2</sub>. It is not necessary to be the film and alternative removal is just performed to the first mask M1 at a next process. Since the third mask M3 should just have an edge on the first mask M1, it is easy mask alignment. As p mold impurity and a becoming impurity, aluminum (it is described as Following aluminum) etc. can be used other than B.

[0035] SiO<sub>2</sub> the third membranous mask M3 -- removing -- a photolithography -- \*\* -- a part of first mask -- M1b -- removing -- a part of first mask -- [this drawing (d)] which leaves M1a. a part of first mask which it left -- M1a is used as a mask and B ion 5a is poured in again. [This drawing (e)]. This is p<sup>+</sup>. It is for embedding field 42 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation 1x10<sup>15</sup>cm<sup>-2</sup>. Acceleration voltage was raised for forming a deep impurity range. As a p mold impurity, aluminum etc. may be used other than B.

[0036] a part of first mask which it left -- M1a is removed and N ion 4a is poured into the whole surface. [This drawing (f)]. 4b is poured-in N atom. This is for concentration control of the n channel field 50, acceleration voltage is 200keV(s) and a dose is abbreviation 1x10<sup>12</sup>cm<sup>-2</sup>. Before this, it is p<sup>+</sup>. Since the deep ion implantation for the embedding field 42 is performed, it is p<sup>+</sup>. B atom is poured into n drift layer 41b of the surface layer which comes on the embedding field 42. Resistance of a surface layer can be stabilized by impregnation of N ion. The high impurity concentration of the surface layer after heat treatment is abbreviation 5x10<sup>15</sup>cm<sup>-3</sup>. It

becomes.

[0037] It is n+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The source field 43, p gate field 44, and p+ Each field of the embedding field 42 is formed [ drawing 3 (a)]. Although diffusion of an impurity hardly breaks out in SiC as stated previously, the depth in which an impurity range is formed is controllable by accommodation of acceleration voltage. For example, p+ The embedding field 42 is made by the layer with a thickness of 0.5 micrometers at focusing on a depth of 0.8 micrometers by having made acceleration voltage high with 400keV(s), and n about 0.5-micrometer drift region 41b is left behind on it. p gate field 44 and n+ The depth of the source field 43 is about 0.2 micrometers.

[0038] To a front face, it is SiO<sub>2</sub> by the CVD method. The film 2 is deposited [this drawing (b)]. It is n+ at RIE form the fourth mask M4 by the photolithography, and using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>). Crevice 47a which arrives at p+ embedding field 42 from the front face of the source field 43 is formed [this drawing (c)]. It is SiO<sub>2</sub> at a photolithography. After forming opening for contact in the film 2 Pattern formation of the aluminium alloy film is vapor-deposited and carried out, and it considers as the source electrode 47 and the gate electrode 46., n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].

[0039] By taking the above manufacture approaches, it was able to consider as the high proof-pressure SiC vertical mold JFET of drawing 1 . SiCJFET of an example 1 -- a part of first mask - the edge of M1b -- n+ the source field 43 specifies -- having -- a part of first mask -- p gate field 44 is prescribed by another edge of M1b, and another partial M1a of the first mask. By partial M1a with the first still more nearly another mask, it is p+. The edge of the embedding field 42 is specified. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. After the pattern formation of the first mask M1, the advantage that the dimension of each impurity range can be checked is also.

[0040] Although the control is very important on application since the die length of a channel field is a main parameter which determines the property of MOSFET, in SiCJFET of this example 1, the n channel field 50 of the lower part of p gate field 44 serves as channel length substantially, channel length is formed with a precision short and sufficient to homogeneity, and the stable property and the high yield are obtained. The on resistance of JFET of 1500V class made as an experiment showed 15m ohm-cm<sup>-2</sup> and a low value.

[0041] Moreover, p+ The embedding field 42 was formed by the ion implantation with high acceleration voltage, the junction depth was written deeply, and high pressure-proofing beyond 1500V has been realized easily. By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 41b, the threshold voltage of MOSFET can be controlled and it can also be referred to as FET of no MARIOFU.

[0042] Some deformation is also considered as the manufacture approach. For example, n+ Reverse is sufficient as the sequence of the ion implantation for forming the source field 43 and p gate field 44. Moreover, the ion implantation for high-impurity-concentration control of the n channel field 50 may be performed first. If it will carry out at low temperature more instead of an elevated temperature which calls an ion implantation 1000 degrees C, the selection width of face of a mask ingredient can extend.

[0043] [Example 2] drawing 4 is the fragmentary sectional view of SiCJFET concerning the second example of this invention. This is the modification of the example 1 of drawing 1 . A

crevice is not formed in a SiC substrate front face in this example, but it is p+ to the surface layer of n drift layer 51b. p+ which arrives at the embedding field 52 Contact field 52a is formed and it is n+ to that front face. The source field 53 and the common source electrode 57 are formed.

[0044] n+ As a mask (it is equivalent to M2 of drawing 2 (b)) in the case of N ion implantation for source field 53 formation, it is n+. The mask which also specifies the outside of the source field 53 is used, still more nearly another mask is used, and it is p+. What is necessary is just to perform B ion implantation for contact field 52a formation. If it does in this way, a crevice cannot be formed but an electrode can be prepared in a substrate front face.

[0045] n+ There is instead of [ no ] in a part of first mask (it being equivalent to M1b of drawing 2 (b)) specifying the inside of the source field 53, and the die length of a channel field is the same as that of SiCJFET of an example 1, the n channel field 60 of the lower part of p gate field 44 has short uniform channel length, it is form with a sufficient precision, and the stable property and the high yield are obtain.

[0046] [Example 3] drawing 5 is the fragmentary sectional view of SiCJFET concerning the third example of this invention. This can also say it also as deformation of SiCJFET of drawing 1 .

The point different from SiCJFET of drawing 1 is a point that the gate electrode 66 touches common to p gate field 64 and the front face of n drift layer 61b. Here, the gate electrode 66 chooses a SiC substrate and a metal which forms the Schottky barrier, for example, Ti, aluminum, Pt, etc.

[0047] At JFET of an example 1, as for p gate field 44, contact is taken only in the part which the gate electrode 46 contacts so that drawing 1 may show. In order to stop this contact resistance small, the touch area had to be enlarged and the magnitude of this contact aperture had restricted the minimum value of the die length of a channel. Since JFET of this example 3 improves this point and the gate electrode 66 touches not only p gate field 64 but the front face of n drift layer 61b, a large contact part can be taken and it becomes possible to design a channel field narrowly.

[0048] It also sets to JFET of this example 3, and is n+. It is the same that the property which a source field carries out self align to the surface layer of p base region, and is formed, and channel length was formed with a uniformly and sufficient precision like JFET of an example 1, and was stabilized is acquired with the sufficient yield. However, the gate electrodes 66 are a SiC substrate and the metal which forms the Schottky barrier, and are not necessarily the same metal as the source electrode 67. Or the gate electrode 66 may be made into a bilayer with the same metal as the metal and the source electrode 67 which carry out Schottky contact. About the process which manufactures this, it is almost almost the same as that of drawing 2 and 3, and explanation is omitted.

[0049] [Example 4] drawing 6 is the fragmentary sectional view of SiCMOSFET concerning the fourth example of this invention. n+ In the wafer with which the laminating of the n drift layer 71b was carried out by epitaxial growth on substrate 71a It is p+ from the front face of n drift layer 71b to a somewhat deep location. The embedding field 72 is formed and it is the p+. It is n+ to the surface layer of upper n drift layer 71b of the embedding field 72. Although the point that the source field 73 is formed is the same as an old example There is nothing and p gate field is p+. The upper part of the embedding field 72 is made into the n channel field 80, and the gate of metal-oxide-semiconductor structure is prepared on the front face.

[0050] That is, the gate electrode layer 76 which consists of a polycrystalline silicon layer through gate oxide 75 is formed on the front face of n drift layer 71b. 79 is an insulator layer of boron phosphorus silica glass (BPSG) which insulates the gate electrode layer 76 and the source electrode 77. n+ There is crevice 77a investigated from the front face of the source field 73, the



front face is met, and it is n+. The source field 73 and p+ The source electrode 77 which contacts common to a front face with the embedding field 72 is formed, and it is n+. The rear face of substrate 71a is contacted and the drain electrode 78 is formed. The dimension of main each part is almost the same as the value stated in the example 1. The thickness of gate oxide 75 is [ the thickness of 1 micrometer and an insulator layer 79 of the thickness of 50nm and the gate electrode layer 76 ] 2 micrometers.

[0051] When this MOSFET is also called ACCUFET and impresses a forward electrical potential difference to the gate electrode layer 76, induction of the accumulation layer is carried out to the surface part of n drift layer 71b of gate electrode layer 76 directly under, and a current flows between the drain electrode 78 and the source electrode 77. Moreover, if a negative electrical potential difference is impressed to the gate electrode layer 76, the current between the drain electrode 78 and the source electrode 77 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 72 and n drift layer 71b, and to hold a big electrical potential difference, and it has structure suitable for high pressure-proofing.

[0052] Drawing 7 (a) thru/or (e) and drawing 8 (a) thru/or (d) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 4 of drawing 6 . A process is explained in order of below. n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 71b of a phosphorus dope with epitaxial growth is prepared on substrate 71a. The high impurity concentration of n drift layer 71b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 71b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [ drawing 7 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0053] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of a polycrystal silicone film. After depositing the film, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, N ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [ these ] [this drawing (b)]. This is n+. It is for source field 73 formation, and acceleration voltage, a dose, etc. are the same as an example 1, and good. this second mask M2 -- not necessarily -- SiO<sub>2</sub> it is not necessary to be -- although -- since it is required to remove leaving the first mask M1 at a next process, unlike the first mask M1, the ingredient which can perform alternative etching is chosen. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, P etc. is used other than N.

[0054] SiO<sub>2</sub> the second membranous mask M2 -- removing -- a photolithography -- a part of first mask -- [this drawing (c)] which pours in the ion used as p mold impurity, for example, B ion 5a, after leaving M1a. This is p+. It is for embedding field 72 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . Acceleration voltage was raised for forming a deep impurity range. As for p mold impurity, aluminum etc. is used other than B.

[0055] a part of first mask which it left -- M1a is removed and N ion 4a is poured in. [This drawing (d)]. This is for high-impurity-concentration control of the n channel field 80, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . It is p+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The embedding field 72 and n+ Each field of the source field 73 and the n channel field 80 is formed [this drawing (e)].

[0056] SiO<sub>2</sub> film which turns into gate oxide 75 by 1200 degrees C and thermal oxidation of 2 hours is formed in a front face, and about 1 micrometer of polycrystal silicon films 1 which serve as a gate electrode layer with a reduced pressure CVD method continuously is deposited [drawing 8 (a)]. It forms by thermal oxidation, and also gate oxide 75 can also form membranes by CVD. As an ingredient of the gate electrode layer 76, molybdenum (Mo) etc. is [ other than polycrystalline silicon ] usable.

[0057] A photoresist is applied, and after carrying out pattern formation of the polycrystal silicon film 1 by the photolithography and considering as the gate electrode layer 76, the insulator layers 79, such as boron phosphorus silica glass (BPSG), are deposited on a front face with a CVD method [this drawing (b)]. It is n<sup>+</sup> at RIE form a pattern by the photolithography and using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>). The front face of the source field 73 to p<sup>+</sup> Crevice 77a which arrives at the embedding field 72 is formed [this drawing (c)].

[0058] After forming opening for contact in an insulator layer 79 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 77 and the gate electrode which is not illustrated. n<sup>+</sup> A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].

MOSFET of this example 4 -- also setting -- a part of first mask -- the edge of M1b -- n<sup>+</sup> The source field 73 is specified and the edge of p<sup>+</sup> embedding field 72 is prescribed by partial M1a with the first another mask. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise.

[0059] Therefore, like JFET of an example 1, about 1.5-micrometer channel length is realized with a uniformly and sufficient precision, and the stable property is acquired with the sufficient yield. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also. By being added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 71b, and considering as the n channel field 80, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU.

[0060] Moreover, since gate oxide 75 is formed on the SiC substrate at the plane, there is no problem of the stress of the electric field in the corner section of the gate oxide seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 80 may be performed first, and reverse order is sufficient as formation with the second mask M2 and the third mask M3.

[0061] n<sup>+</sup> In the case of N ion implantation for source field 73 formation, it is n<sup>+</sup>. The mask which specifies the outside of the source field 73 is used, still more nearly another mask is used, and it is p<sup>+</sup>. If B ion implantation for contact field 52a formation is performed, crevice 77a cannot be formed but an electrode can be prepared in a substrate front face. In that case The die length of a channel field is formed in homogeneity with a sufficient precision like SiCMOSFET of an example 4, and the stable property and the high yield are obtained.

[0062] [Example 5] drawing 9 is the fragmentary sectional view of SiCMOSFET concerning the fifth example of this invention. n<sup>+</sup> It is p<sup>+</sup> to a somewhat deep location from the front face of n drift layer 81b deposited with epitaxial growth on substrate 81a. The embedding field 82 is formed and it is p<sup>+</sup>. The p base region 82 is formed in the surface layer of upper n drift layer 81b of the embedding field 82, and it is n<sup>+</sup> alternatively in the upper part. The source field 83 is

formed. And the part of the edge of the p base region 82 is n+. It is so characteristic that it keeps away from the source field 83 that the junction depth is shallow almost linearly. Moreover, it is p+ to a part deeper than the p base region 82 so that the p base region 82 may be overlapped in part. Contact field 82a is formed. n+ The upper part of the p base region 82 of a part in which the source field 83 is not formed is made into the n channel field 90, and the gate of the same metal-oxide-semiconductor structure as MOSFET of drawing 6 is prepared on it. That is, the gate electrode layer 86 which consists of a polycrystalline silicon layer through gate oxide 85 is formed. 89 is the insulator layer of BPSG which insulates a gate electrode layer and the source electrode 87. n+ From the front face of the source field 83, there is investigated crevice 87a and it is n+. The source field 83 and p+ It contacts common to a front face with the contact field 82, and the source electrode 87 is formed, and it is n+. The rear face of substrate 81a is contacted and the drain electrode 88 is formed.

[0063] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of  $1 \times 10^{18} \text{cm}^{-3}$  in 350 micrometers in 3 and thickness and n drift layer 41b is  $1 \times 10^{16} \text{cm}^{-3}$  10 micrometers in 3 and thickness. Spacing between 3 and a junction depth of 1.5 micrometers of  $5 \times 10^{16} \text{cm}^{-3}$ , and the p base region 82 of both sides of the highest high impurity concentration of the p base region 82 is about 6 micrometers. n+ The high impurity concentration of the source field 43 is  $1 \times 10^{19} \text{cm}^{-3}$  3 and a junction depth of 0.2 micrometers, and width of face is about 5 micrometers and p+. The highest high impurity concentration of the contact field 82 is [ the high impurity concentration of about 5 micrometers and the n channel field 90 of 3 and a junction depth of 2.0 micrometers of  $1 \times 10^{19} \text{cm}^{-3}$ , and width of face ]  $5 \times 10^{15} \text{cm}^{-3}$  3 and a junction depth of 0.5 micrometers. n+ Spacing between the edge of the source field 83 and the edge of the p base region 82 is about 2 micrometers. The depth of crevice 87a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 30 micrometers. The thickness of gate oxide 85 is [ the thickness of 1 micrometer and an insulator layer 89 of the thickness of 50nm and the gate electrode layer 86 ] 2 micrometers.

[0064] Drawing 10 (a) thru/or (e) and drawing 11 (a) thru/or (e) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 5 of drawing 9. A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 81b of a phosphorus dope with epitaxial growth is prepared on a substrate. On the front face of n drift layer 81b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1.

[0065] It is important especially in the case of this patterning to form the taper section 8 in the edge of the first mask M1 over 1-2 micrometers. This is because channel length is controlled by the include angle of the taper section 8 of the first mask M1 in the ion implantation for the next p base region formation. Therefore, this cone angle must be captured and decided to be a predetermined design. And this include angle is controllable by choosing the etching conditions at the time of etching the thin film of the first mask 1 by plasma etching etc. Or a loose taper will be obtained, if an ion implantation is carried out to the upper part of a thin film, the damage is given to it and it carries out only near the front face that it is easy to be etched. There is also the approach of controlling a taper angle by controlling the dose of the ion implantation in that case.

[0066] The ion, for example, boron (B) ion 5a, which serves as p mold impurity by using the first mask M1 as a mask is poured in [ drawing 10 (a)]. 5b is poured-in B atom. This is for p base region 82 formation, acceleration voltage is 300keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ .



Acceleration voltage was raised for forming a deep impurity range. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow almost linear gradually as thickness of the mask [ first ] M1 increases, and an impurity atom carries out distribution as shown in drawing. If thickness of the first mask M1 is made to some extent thin, an impurity impregnation field does not arrive at even a front face, but can be made into the field of an embedding mold. As for p mold impurity, aluminum etc. is used other than B. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0067] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using the first same mask M1 as a mask is poured in [this drawing (b)]. 4b is poured-in n atom. This is for n+ source field 83 formation, and the 100keV(s) as an example 1 with the same acceleration voltage etc. and a dose are good at abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . In the field which does not have the first mask M1 in this case, either, an impurity is poured in deeply, if the first mask M1 becomes thick, it will become shallow gradually, and an impurity atom carries out distribution as shown in drawing. However, since acceleration voltage is made low, the field poured in differs from the impregnation field of B ion. If the include angle of the taper section 8 is the same, spacing of the impregnation field of p mold impurity and the impregnation field of n mold impurity will become fixed.

[0068] It is SiO<sub>2</sub> by the heat CVD method on the first mask M1 of a polycrystal silicone film. The film 2 is deposited [this drawing (c)]. After forming a sidewall 9 in the side of \*\* and the taper section 8 of the first mask M1 carrying out overall etching by RIE, the ion used as p mold impurity, for example, B ion 5a, is poured into the field specified by these first masks M1 and the sidewall 9 [this drawing (d)]. This is high-concentration p+. It is for contact field 84 formation, and acceleration voltage, 400keV, and a dose are abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . As a p mold impurity, aluminum etc. is used other than B.

[0069] After removing the first mask M1 and a sidewall 9, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field 90, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . Thereby, a threshold is controllable. Each field is formed by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity [ drawing 11 (a)]. Thus, p base region 82sn+ The source field 83 can be shifted and formed.

[0070] Heat SiO<sub>2</sub> with a thickness of 50nm it is thin to gate oxide 85 on a front face with 1200 degrees C and thermal oxidation of 2 hours The film 6 is formed, and about 1 micrometer of polycrystal silicone films 1 is continuously deposited with a reduced pressure CVD method [this drawing (b)]. It forms by thermal oxidation, and also gate oxide 85 can also form membranes by CVD. After applying a photoresist, carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 86, with a CVD method, the insulator layers 89, such as boron phosphorus silica glass (BPSG), are deposited on a front face, and a pattern is formed in it by the photolithography [this drawing (c)].

[0071] At RIE using the mixed gas of carbon tetrafluoride (CF<sub>4</sub>) and oxygen (O<sub>2</sub>), it is p+ from the front face of n+ source field 83. Crevice 87a which reaches contact field 82a is formed [this drawing (d)]. After forming opening for contact in an insulator layer 89 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 87 and the gate electrode which is not illustrated [this drawing (e)]. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed.

[0072] In MOSFET of this example 5, the edge of n+ source field 83 and the p base region 82 is

prescribed by making the edge of the first mask 1 into the shape of a taper, and changing the acceleration voltage in the case of impregnation of p mold impurity and n mold impurity. That is, the channel length who is spacing between both is prescribed by the taper section 8 of the first mask M1. Thus, since the impurity range is prescribed by only the first mask, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, does not occur.

[0073] Therefore, channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield. Moreover, if the include angle of the taper section 8 of the first mask M1 is changed, both spacing, i.e., the die length of a channel field, can be controlled freely, and the balance of on resistance and pressure-proofing will also tend to take it. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also.

[0074] By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 81b, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 90 may be performed first. Moreover, impregnation and n+ of B ion for the p base region 82 Reverse is sufficient as the order of impregnation of N ion for source field 83 formation. A sidewall field is formed first and it is p+. The ion implantation for contact field 84 formation may be performed.

[0075] Since gate oxide 85 is formed on the SiC substrate also in this example at the plane, there is no problem of the stress of the electric field in the gate oxide corner section seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Moreover, at this example, it is p+. It is n+, although contact field 82a was embedded and being considered as the field of a mold. In the case of N ion implantation for source field 83 formation, it is n+. The mask which specifies the outside of the source field 83 is used, and it is p+. If contact field 82a is made to arrive at even a front face by multiplex impregnation, the source electrode 87 can be formed in a substrate front face, and there will be no need of forming crevice 87a.

[0076] [Example 6] drawing 12 (a) thru/or (e) are the fragmentary sectional views near the front face of the order of a production process for explaining the another manufacture approach of the almost same SiCMOSFET as SiCMOSFET of drawing 9. A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 91b of a phosphorus dope with epitaxial growth is prepared on a substrate. The high impurity concentration of n drift layer 91b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 91b, it is SiO<sub>2</sub> with a thickness of about 2 micrometers by the plasma-CVD method. The film 2 is deposited, a pattern is formed by the photolithography, and it considers as the third mask M3.

[0077] The ion, for example, B ion 5a, which serves as p mold impurity by using the third mask M3 as a mask is poured in [ drawing 12 (a)]. 5b is poured-in B atom. This is high-concentration p+. It is for contact field 94 formation, and acceleration voltage, 400keV, and a dose are abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . As a p mold impurity, aluminum etc. is used other than B.

[0078] Next, CF<sub>4</sub>+H<sub>2</sub> It considers as the first mask M1 which carried out etchback of the third mask M3, and made the edge the shape of a taper over 1-2 micrometers by plasma etching using gas [this drawing (b)]. At this time, the whole thickness also becomes thin and thickness is set to about 1 micrometer. In the ion implantation for the next p base region formation, a channel is controlled by the cone angle of the edge of the first mask by this like the time of SiCMOSFET of

an example 5.

[0079] The ion, for example, B ion 5a, which serves as p mold impurity by using as a mask the first mask M1 which made the edge the shape of a taper is poured in [this drawing (c)]. This is for p base region 92 formation, acceleration voltage is 300keV(s) and a dose is abbreviation  $1 \times 10^{15} \text{cm}^{-2}$ . In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow gradually as thickness of the mask [first] M1 increases, and an impurity atom carries out distribution as shown in drawing.

[0080] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using as a mask the first mask M1 which made the same edge the shape of a taper is poured in [this drawing (d)]. This is n+. It is for source field 93 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation  $5 \times 10^{15} \text{cm}^{-2}$ . Since acceleration voltage is made low, the field poured in differs from the impregnation field of p mold impurity.

[0081] After removing the first mask M1, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field of the surface layer of n drift layer 91b, acceleration voltage is 200keV(s) and a dose is abbreviation  $1 \times 10^{12} \text{cm}^{-2}$ . Thereby, a threshold is controllable. After this, activation of the impurity poured in after drawing 10 (a), formation of an electrode, etc. are performed.

[0082] Since back dirty [of the third mask M3] was carried out and it considered as the first mask M1 when taking this approach, it is not necessary to form a mask ingredient anew. And since the include angle of the taper section also becomes homogeneity and spacing of the p base region 92 and n source field 93 is specified, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. And channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield.

[0083] Some deformation is also considered as the manufacture approach. For example, a reverse order is sufficient as impregnation [drawing 12 (c)] of p mold impurity ion for p base region formation, and impregnation [drawing 12 (d)] of n mold impurity ion for n source field formation, and the ion implantation for high-impurity-concentration control of an n channel field [drawing 12 (e)] may be performed first.

---

[Translation done.]



**\* NOTICES \***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.

2. \*\*\*\* shows the word which can not be translated.

3. In the drawings, any words are not translated.

---

**DESCRIPTION OF DRAWINGS**

---

[Brief Description of the Drawings]

[Drawing 1] The fragmentary sectional view of MOSFET of the first example of this invention

[Drawing 2] (a) - (f) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of JFET of an example 1.

[Drawing 3] (a) - (d) is the fragmentary sectional view of the order of a process of JFET of the example 1 following drawing 2 (f).

[Drawing 4] The fragmentary sectional view of JFET of an example 2

[Drawing 5] The fragmentary sectional view of JFET of an example 3

[Drawing 6] The fragmentary sectional view of MOSFET of an example 4

[Drawing 7] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 4.

[Drawing 8] (a) - (d) is the fragmentary sectional view of the order of a process of MOSFET of the example 3 following drawing 7 (e).

[Drawing 9] The fragmentary sectional view of MOSFET of an example 5

[Drawing 10] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 5.

[Drawing 11] (a) - (e) is the fragmentary sectional view of the order of a process of MOSFET of the example 5 following drawing 10 (e).

[Drawing 12] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 6.

[Drawing 13] The fragmentary sectional view of the conventional JFET

[Drawing 14] The fragmentary sectional view of the conventional MOSFET

[Drawing 15] The fragmentary sectional view of another conventional MOSFET

[Description of Notations]

M1, M1a, M1b The first mask

M2 The second mask

M3 The third mask

1 Polycrystal Silicone Film

2 SiO<sub>2</sub> Film

3 Insulator Layer

4a Nitrogen ion

4b Nitrogen atom

5a Boron ion

5b Boron atom

6 Thermal Oxidation Film

7 Crevice

8 Taper Section  
9 Sidewall  
10 P Mold Substrate  
11a n+ Drain field  
11b, 21b, 31b, 41b, 51b, 61b, 71b, 81b n drift layer  
13, 23, 33, 43, 53, 63, 73, 83 n+ Source field  
14, 44, 54, 64 p gate field  
16, 46, 66 Gate electrode  
17, 27, 37, 47, 57, 67, 77, 87 Source electrode  
18, 28, 38, 78, 88 Drain electrode  
19, 39, 49, 59, 69, 79, 89 Insulator layer  
20, 30, 40, 50, 60, 70, 80, 90 Channel field  
21a, 31a, 41a, 71a, 81a n+ Drain layer  
22, 42, 52, 72 p+ Embedding field  
25, 35, 75, 85 Gate oxide  
26, 36, 76, 86 Gate electrode layer  
32 82 p base region  
37a, 47a, 77a, 87a Crevice  
52a, 82a p+ Contact field

---

[Translation done.]